

MODELING BAND-PASS SIGMA-DELTA MODULATORS IN SIMULINK

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Abstract: In this paper we present a complete set of behavioral SIMULINK models for the simulation of switched-capacitor band-pass sigma-delta (BPΣΔ) modulators. The models include most of the non-idealities which affect the performance of these circuits, such as sampling jitter, kT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages). With the proposed models it is possible to accurately predict with fast simulations the signal-to-noise and distortion ratio and the linearity of any BPΣΔ modulator.

Keywords: Sigma-delta modulators, A/D converter modeling, Behavioral modeling

1. INTRODUCTION

Direct analog-to-digital (A/D) conversion of band-limited signals centered at Intermediate Frequency (IF) by oversampling converters is becoming very popular in telecommunication systems. Band-pass Sigma-Delta (BPΣΔ) modulators are representing the reference front-end architecture for Amplitude Modulation (AM), Quadrature Amplitude Modulation (QAM) and Frequency Modulation (FM) systems. While maintaining all the well-known advantages of conventional oversampling converters (namely simplicity, robustness, and linearity), BPΣΔ allow direct digital demodulation of the converted signal. Since no tuning is required, long-term stability of the system is also increased.

After early RL-based discrete modulators, the research focused on the integration of complete BPΣΔ modulators using Switched-Capacitor (SC) biquadratic cells [1, 2], as shown in Fig. 1 (second-order BPΣΔ modulator, fourth order loop). As in conventional low-pass SC ΣΔ sigma-delta modulators, to achieve the desired signal-to-noise ratio and linearity, we have typically to optimize a large set of parameters, including the performances of the building blocks. In view of the inherent non-linearity of the ΣΔ modulator loop this optimization process has to be carried out with behavioral simulations. Therefore, in this paper we present a complete set of SIMULINK models, which allow us to perform exhaustive behavioral simulations of any BPΣΔ modulator taking into account most of the non-idealities, such as sampling jitter, kT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages) [5]. With these models it is possible to accurately predict with a fast simulation time the signal-to-noise and distortion ratio (SNDR) and the linearity performance of any BPΣΔ modulator (including the third order intermodulation product, IP_3 , which is particularly important in telecommunication systems).

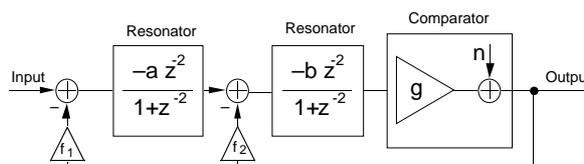


Figure 1. Block diagram of a second-order band-pass sigma-delta modulator

2. BAND-PASS SIGMA-DELTA MODULATOR MODELING

Fig. 2 shows the block diagram of a second-order BPΣΔ modulator implemented using the proposed SIMULINK models. In the circuit only the non-idealities of the first resonator are considered, since their effects are not attenuated by the noise shaping. The proposed SIMULINK model includes the most significant non-ideality of a sigma-delta modulator, namely clock jitter, switch thermal noise (kT/C), and operational amplifier non-idealities (slew-rate, finite bandwidth, finite gain, thermal noise and finite output swing). Each effect is modeled with a SIMULINK block or MATLAB function.

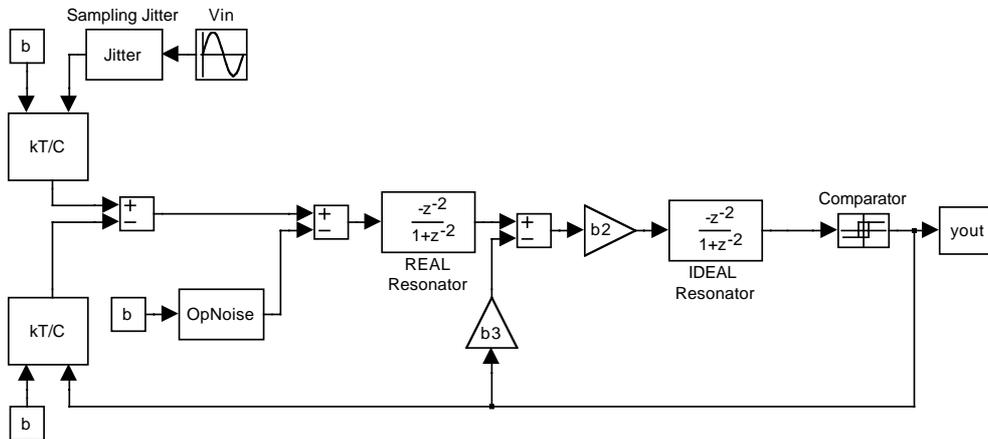


Figure 2. Block diagram of a second-order band-pass sigma-delta modulator implemented using the proposed SIMULINK models

2.1. Clock Jitter

The effect of clock jitter on an SC BPΣΔ modulator can be calculated in a fairly simple manner, since the operation of a SC circuit depends on complete charge transfers during each of the clock phases. In fact, once the analog signal has been sampled the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal. This means also that the effect of clock jitter on a BPΣΔ modulator is independent of the structure or order of the modulator.

Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal of the modulator. The error introduced when a sinusoidal signal with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by

$$x(t + \delta) - x(t) \approx 2\pi f_{in} \delta A \cos(2\pi f_{in} t) = \delta \frac{d}{dt} x(t) . \quad (1)$$

This effect can be simulated with SIMULINK by using the model shown in Fig. 3, which implements Eqn. (1). Here, we assumed that the sampling uncertainty δ is a Gaussian random process with standard deviation $\Delta\tau$. Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power spectral density from 0 to $f_s/2$, with a total power of $(2\pi f_{in} \Delta\tau A)^2 / 2$. In this case, the total error power will be reduced by the oversampling ratio.

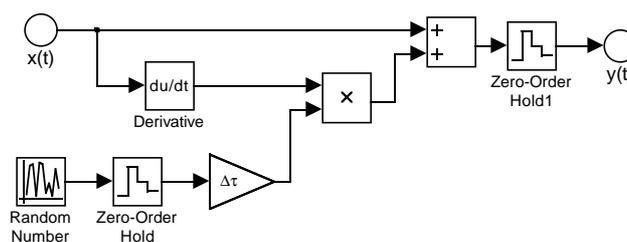


Figure 3. Modeling a random sampling jitter

2.2. Thermal Noise

The most important noise sources affecting the operation of an SC BPΣΔ modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifier. The total thermal noise power of the circuit is the sum of the switch noise power and the operational amplifier noise power. Because of the large in-band gain of the first resonator, whose schematic is shown in Fig. 4 [1], the noise performance of a BPΣΔ modulator is determined mainly by the switch and operational amplifier noise of the input stage. In the models the coefficient b represents the resonator gain (ratio between the sampling capacitance C_s and the feedback capacitor C_f , as shown in Fig. 4).

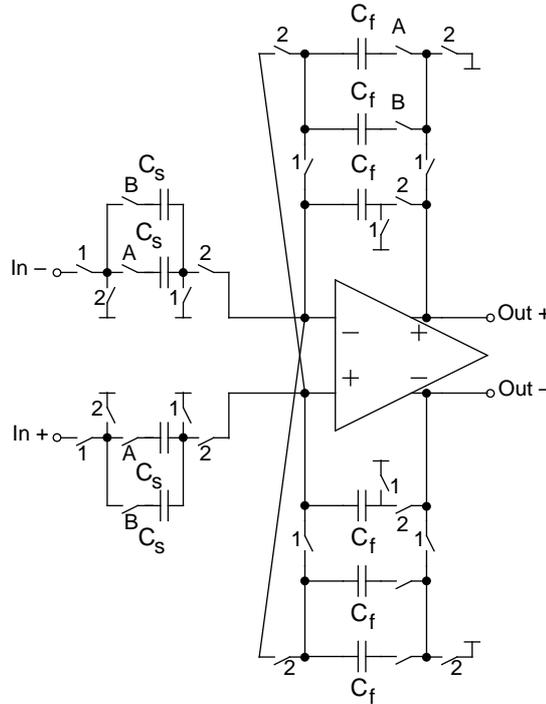


Figure 4. Schematic of a SC biquadratic resonator

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of the operational amplifiers. Therefore, it must be taken into account for both the switches and the operational amplifiers in a SC circuit. The sampling capacitor C_s in a SC resonator is in series with a switch, with finite resistance R_{on} , that periodically opens, sampling a noise voltage onto the capacitor. The total noise power can be found evaluating the integral [3]

$$e_T^2 = \int_0^{\infty} \frac{4kTR_{on}}{1 + (2\pi f R_{on} C_s)^2} df = \frac{kT}{C_s} \quad (2)$$

where k is the Boltzman constant, T the absolute temperature and the resistance is modeled with a noise source in series with power $4kTR_{on} \Delta f$. The switch thermal noise voltage e_T (usually called kT/C noise) is superimposed to the input voltage $x(t)$ leading to

$$y(t) = [x(t) + e_T(t)]b = \left[x(t) + \sqrt{\frac{kT}{bC_f}} n(t) \right] b \quad (3)$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation, while b is the resonator gain. Eqn. (3) is implemented by the model shown in Fig. 5.

Since the noise is aliased in the band from 0 to $F_s/2$, its final spectrum is white with a spectral density

$$S(f) = \frac{2kT}{F_s C_s} \quad (4)$$

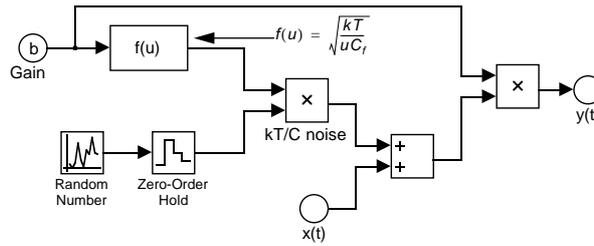


Figure 5. Modeling switches thermal noise (kT/C block)

Typically the first resonator will have two switched input capacitors, one carrying the signal and the other providing the feedback from the modulator output, each of them contributing to the total noise power.

Fig. 6 shows the model used to simulate the effect of the operational amplifier noise. Here, V_n represents the total *rms* noise voltage referred to the operational amplifier input. Flicker ($1/f$) noise, wide-band thermal noise and dc offset contribute to this value. The total operational amplifier noise power V_n^2 can be evaluated, through transistor level simulation.

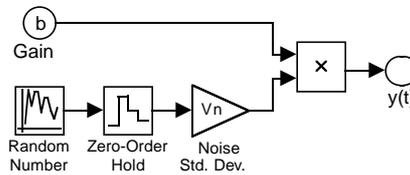


Figure 6. Operational amplifier noise model

2.3. Resonator Non-Idealities

Analog circuit implementations of an SC resonator deviate from the ideal behavior due to several non-ideal effects. One of the major causes of performance degradation in SC BPΣΔ modulators, indeed, is due to incomplete transfer of charge in the SC resonators. This non-ideal effect is a consequence of the operational amplifier non-idealities, namely finite gain and bandwidth, slew rate and saturation voltages. These will be considered separately in the following paragraphs. Fig. 7 shows the model of the real resonator including all the non-idealities.

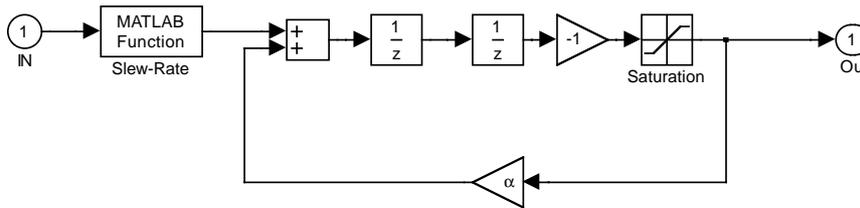


Figure 7. SIMULINK model of the basic SC resonator (real resonator)

The in-band gain of the resonator described by Eqn. (5) is infinite. In practice, however, the gain is limited by circuit constraints. The consequence of this resonator “leakage” is that only a fraction α of the previous output of the resonator is added to each new input sample (parameter α in Fig. 7). The transfer function of the resonator with leakage and the dc gain become

$$H(z) = -\frac{z^{-2}}{1 + \alpha z^{-2}} \text{ and } H_0 = H(i) = \frac{1}{1 - \alpha} . \tag{5}$$

The finite bandwidth and the slew-rate of the operational amplifier are modeled in Fig. 7 with a building block placed in front of the resonator which implements a MATLAB function. The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain [4]. The evolution of the output node of a SC resonator during the n th integration period is

$$v_0(t) = v_0(nT - T) + \alpha V_s \left(1 - e^{-\frac{t}{\tau}} \right), \quad nT - \frac{T}{2} < t < nT \quad (6)$$

where $V_s = V_{in}(nT - T/2)$, α is the resonator leakage and $\tau = 1/(2\pi \text{ GBW})$ is the time constant of the operational amplifier (GBW is the unity gain frequency of the operational amplifier when loaded by C_f). The slope of this curve reaches its maximum value when $t = 0$, resulting in

$$\left. \frac{d}{dt} v_0(t) \right|_{max} = \alpha \frac{V_s}{\tau}. \quad (7)$$

We must consider now two separate cases:

1. The value specified by Eqn. (7) is lower than the operational amplifier slew-rate, SR . In this case there is not slew-rate limitation and the evolution of v_0 fits Eqn. (6).
2. The value specified by Eqn. (7) is larger than SR . In this case, the operational amplifier is in slewing and, therefore, the first part of the temporal evolution of v_0 ($t < t_0$) is linear with slope SR . The following equations hold (assuming $t_0 < T$):

$$t \leq t_0 \quad v_0(t) = v_0(nT - T) + SRt, \quad (8)$$

$$t > t_0 \quad v_0(t) = v_0(t_0) + (\alpha V_s - SRt_0) \left(1 - e^{-\frac{t-t_0}{\tau}} \right). \quad (9)$$

Imposing the condition for the continuity of the derivatives of Eqn. (8) and Eqn. (9) in t_0 , we obtain

$$t_0 = \frac{\alpha V_s}{SR} - \tau. \quad (10)$$

If $t_0 \geq T$ only Eqn. (8) holds. The MATLAB function in Fig. 7 implements the above equations to calculate the value reached by $v_0(t)$ at time T , which will be different from V_s due to the gain, bandwidth and slew-rate limitations of the operational amplifier. The slew-rate and bandwidth limitations produce harmonic distortion reducing the total signal-to-noise and distortion ratio ($SNDR$) and the IP_3 performance of the $BP\Sigma\Delta$ modulator.

The dynamic of signals in a $BP\Sigma\Delta$ modulator is a major concern. It is therefore important to take into account the saturation levels of the operational amplifier used. This can be done easily in SIMULINK using the saturation block inside the feedback loop of the resonator, as shown in Fig. 7.

3. RESULTS

To validate the proposed models of the various non-idealities affecting the operation of an SC $BP\Sigma\Delta$ modulator, we performed several simulations with SIMULINK on the second-order modulator shown in Fig. 2. The simulation parameters used are summarized in Tab. 1 and corresponds to the specifications of a $BP\Sigma\Delta$ modulator for digital radio. A minimum $SNDR$ of 55 dB (i.e. a resolution of 9 bits) is required for this kind of application.

Table 1. Simulation parameters

<i>Parameter</i>	<i>Value</i>
Signal bandwidth	BW = 200 kHz
Oversampling frequency	$F_s = 42.8$ MHz
Carrier frequency	$F_c = 10.7$ MHz
Oversampling ratio	$R = 107$
Samples number	$N = 65536$
Resonator gains	$b = b_2 = 0.125, b_3 = 0.25$

Tab. 2 compares the total $SNDR$ and the corresponding equivalent resolution in bits of the ideal modulator, which are the maximum obtainable with the architecture and parameters used, with those achieved with the same architecture when one single limitation at a time is introduced.

Table 2. Simulation results

<i>Resonator Non-Ideality</i>	<i>SNDR [dB]</i>	<i>Resolution</i>
Ideal modulator	82.9	13.48 bits
Sampling jitter ($\Delta\tau = 8$ ns)	64.2	10.37 bits
Switches (kT/C) noise ($C_s = 0.5$ pF)	79.9	12.98 bits
Input-referred operational amplifier noise ($V_n = 4.4$ mV _{rms})	58.4	9.42 bits
Finite gain ($H_0 = 711$)	82.6	13.43 bits
Finite bandwidth and slew-rate ($GBW = 250$ MHz, $SR = 280$ V/ μ s)	82.9	13.48 bits
Saturation voltages ($V_{max} = \pm 1$ V)	82.9	13.48 bits
All the non-idealities	57.2	9.21 bits
Measured on integrated prototype	56.0	9.00 bits

The simulated IP_3 considering all of the non-idealities is -57.5 dB with two 0.5 V input tones. The results obtained from SIMULINK simulations are in pretty good agreement with the performance measured on an integrated prototype.

The baseband power spectral densities of the BP $\Sigma\Delta$ output bitstream obtained in the simulations with and without the non-idealities are shown in Fig. 8.

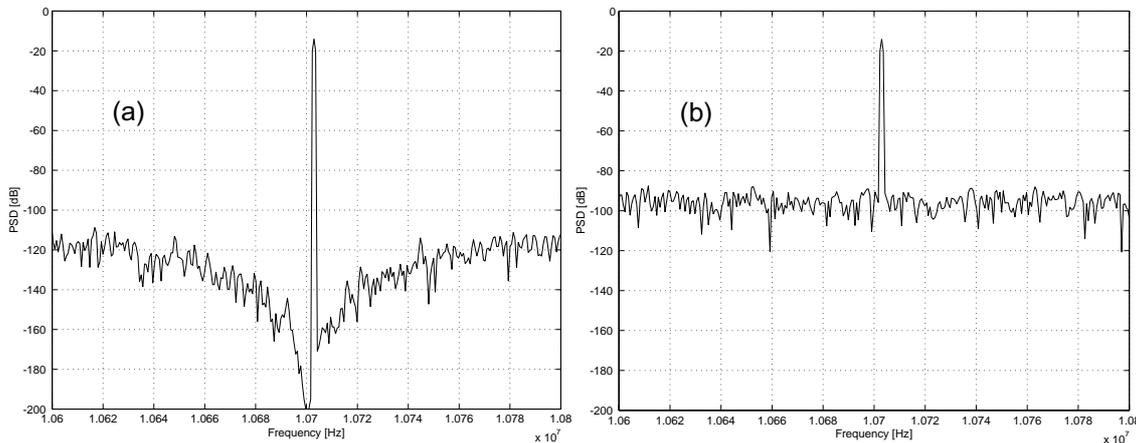


Figure 8. Baseband power spectral densities of the BP $\Sigma\Delta$ output bitstream obtained in simulation with (b) and without (a) the non-idealities

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