XVI IMEKO World Congress
Measurement - Supports Science - Improves Technology - Protects Environment ... and Provides Employment - Now and in the Future
Vienna, AUSTRIA, 2000, September 25-28

DESIGN OF ADC HISTOGRAM TEST: A PRACTICAL CASE

Giovanni Chiorboli
Dipartimento di Ingegneria dell'Informazione, Università di Parma
Parco Area delle Scienze 181/A, 43100 Parma, Italy

Abstract: In this paper, the results of the most recent studies on the sinewave histogram test are considered. Particular emphasis is dedicated to the choice of the values that the test parameters must assume for obtaining a specified measurement uncertainty. Finally, a practical example of how to organize the test of a high-speed, 12-bit converter is proposed, and some results are given which validate the theory.
Keywords: Analog-to-Digital converter, Histogram test, Uncertainty.

1 INTRODUCTION

Code histogram test is a relatively well-known technique for measuring the conversion characteristic of A/D converters (ADCs) and the related parameters such as integral (INL) and differential (DNL) nonlinearities in dynamic conditions. In this technique a high purity sinewave feeds the ADC input and a large number of output codes is collected so as to built a code histogram. The conversion characteristic is then estimated by comparing the measured code histogram and the probability distribution function (PDF) of the input sinewave that is supposed to be ideally pure. Consequently, several causes may affect the measurement accuracy, such as distortion of the input sinewave and random noise which can modify the PDF of the signal, in addition to the finite number of samples used for building the histogram.

The principal error contributions have been originally analyzed by Blair [1] which provided some line guides for a well designed histogram test. These results, included in the IEEE documents and standards [2, 3], have been recently reconsidered with particular care to the effects of the frequency resolution of the signal and clock sources [4, 5] and of the phase noise between them [4]. Moreover, [6, 4] better explain how to estimate measurement uncertainty in accordance with [7]. The last version of the DYNAD draft document [8] summarizes the previous results and, as a consequence, reports some slightly different equations with respect to [2, 3].

The intention of this paper is that of briefly summarizing and verifying with physical experiments the last results of the theory. In fact, to author's knowledge, no results are reported in literature about an experimental validation of the cited analyses. To this aim, the test of a 12-bit, 100MSa/s pipeline ADC, stimulated by an input sinewave at approximately 70MHz, will be discussed. This allows explaining how to organize the test and what are the most relevant contribution to measurement uncertainty in a practical experiment.

2 STATE OF THE ART

Let consider as a typical example of test setup, the block diagram drawn in Fig.1. It consists of two low phase-noise synthesizers which are phase-locked to the same reference signal. The two synthesizers

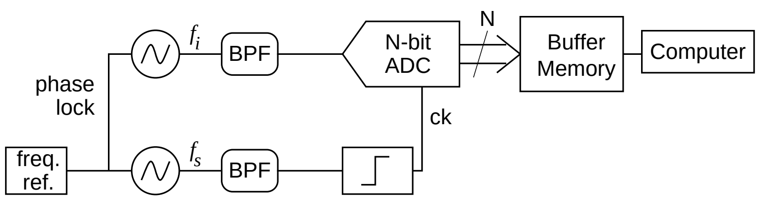

Figure 1: Schematic diagram of the test setup.

provide the analog and the clock signals to a N-bit ADC. Since the analog stimulus is usually represented by

$$v(t) = A\cos(\omega t + \phi) + C \tag{1}$$

particular care has to be taken in filtering out harmonics, additive and phase noise. Finally, R records of output data containing M samples each, are collected and organized in an histogram, which is processed for obtaining the estimates of the transition levels. To minimize the total number of samples, the ratio of the signal over sampling frequencies is chosen so as to collect an integer number of periods within a single record, i.e. $\rho \triangleq f_i/f_s = J/M$, where J and M are mutually prime integer numbers. The transition level between the codes $k-1$ and k is estimated as

$$\hat{T}_k = C - A\cos(\pi H_{k-1}), \quad k = 1, \cdots, 2^N - 1, \tag{2}$$

where H_k represents the k^{th} bin of the cumulative histogram of the ADC output codes, normalized to the total number of samples MR.

As stated before, (2) is based on the assumption that the input signal is a perfectly pure and noiseless sinusoid and that infinite samples are collected to form the histogram. However, in a real environment both distortion and additive noise are present and contribute to the PDF of the signal experienced by the ADC. The change of the PDF with respect to that of a pure sinusoid, systematically acts on the obtained estimation of T_k. At the same time, $\hat{T}_k$ can be modeled as a random variable because of the presence of additive and phase noise and since the initial phase ϕ varies across each record. Therefore, both systematic and random effects have to be considered in order to evaluate their contribution to the measurement uncertainty.

2.1 Systematic effects

The signal amplitude A is preferably chosen so as to slightly overdrive the ADC, since overdriving reduces the systematic effects of the additive noise on the INL and DNL estimates [1].

Two different formulations are reported in [2, 3] and in [8] about the required amount of overdrive. In the present work reference is made to [8], since the reported equations better adhere to the original analysis [1]. Let define the overdrive V_{OD} as the absolute difference between the negative peak value of the input sinewave and the first transition level T_1 and consider that the input signal has to be centered with respect to the ADC's range. If E_{Wpdf} represents the maximum admitted contribution of additive noise to the systematic error in DNL measurements, it is required that

$$V_{OD} \geq \max\left\{3\sigma_{add},\ \sigma_{add}\sqrt{1.43\ \frac{3}{8E_{Wpdf}}}\right\} \tag{3}$$

where σ_{add} is the RMS value of the input referred additive noise.

A similar equation can be used for ensuring that the additive noise contribution to the systematic error in the INL measurements is lower than E_{INLpdf}. It turns out that

$$V_{OD} \geq \max\left\{2\sigma_{add},\ 1.28\ \frac{\sigma_{add}^2 2^N}{V_{rir}E_{INLpdf}}\right\} \tag{4}$$

where V_{rir} is the reduced input range of the ADC in input units.

Harmonic distortion contributes to systematic error mainly in INL measurements since it has a negligible effect on DNL measurements in the presence of a little overdrive [1, 8]. Therefore, the sum of the amplitudes A_i of the harmonic terms has to be below the maximum admitted contribution of distortion to the systematic error $E_{INLdist}$, expressed in LSB, that is

$$\frac{\sum_{i=2}^{h} A_i}{A} \leq \frac{E_{INLdist}}{2^{N-1}} \tag{5}$$

This requirement seems to be slightly restrictive since the phasors associated to the harmonics are probably not equally directed. Therefore (5) does not completely agree with the line-guides to the expression of the uncertainty reported in [7]. Anyway, in the practical cases one harmonic dominates the others and therefore it is not so important to establish how to combine the contribution of the various terms A_i. For instance, to evaluate the INL of a 14 bit ADC with a systematic error below $E_{INLdist} = 0.2$ LSB, the highest harmonic has to be lower than -92dBc.

Notice that, while in general the systematic effect of additive noise can be made negligible by overdriving, the effect of the input distortion cannot be reduced without improving the test hardware.

2.2 Random effects

Random effects are due to the finite number of samples used to build the histogram. In practical case, the number of samples to be acquired for achieving a desired tolerance on the estimated $\hat{T}_k$ becomes relevant. As described above, the two synthesizers must be phase-locked and f_i and f_s have to be chosen so as to acquire an integer number of periods in a record for minimizing the total number of samples. In fact, coherent sampling guarantees that the phase of the sampled data is uniformly distributed between 0 and 2π.

Even in this case and neglecting random noise, the number of counts in each histogram bin can be modeled as a random variable because the initial phase ϕ varies from a record to the other. Since it can be demonstrated that the variance of the number of counts, σ_c^2, is, in the worst case, bounded by 0.25 [4], the expected variance of $\hat{T}_k$ is given by

$$\sigma^2_{\hat{T}_k} = 0.25\,\frac{\pi^2}{M^2}\,\left[A^2 - \overline{T}_k^2\right], \quad k = 1, \cdots, 2^N - 1, \tag{6}$$

where $\overline{T}_k \triangleq T_k - C$ is the centered transition level [6].

However, a perfect-coherent sampling cannot be obtained because of the phase-noise between the two synthesizers and the finite frequency resolution of the two instruments. As a consequence, the true ratio between f_i and f_s usually differs from the constraint $\rho = J/M$ and (6) can underestimate $\sigma^2_{\hat{T}_k}$ if this difference is too large. In [5], authors analyzed the effects of the finite frequency resolution, which is responsible for the mean value of the error in the frequency ratio, $\Delta\rho$. They demonstrated that the contribution of $\Delta\rho$ to the variance of the counts in each histogram bin, σ_c^2, is in any case bounded by 0.25 when

$$\frac{|\Delta\rho|}{\rho} \le \frac{1}{2JM} \tag{7}$$

and that equation (6) can be correctly used if (7) is verified.

Additive noise contributes to the variance of $\hat{T}_k$ as reported in [1], i.e.

$$\sigma^2_{\hat{T}_k} = 1.13\,\frac{\pi}{2M}\,\sqrt{A^2 - \overline{T}_k^2}\;\sigma_{add} \tag{8}$$

Finally, the phase noise between the two synthesizers, combined with the aperture uncertainty of the ADC under test, acts as an additive noise superimposed to the input signal with standard deviation $\sigma_\phi\sqrt{A^2 - \overline{T}_k^2}$, where σ_ϕ is the standard deviation of the phase noise [4]. Its contribution to the variance of $\hat{T}_k$ is so given by

$$\sigma^2_{\hat{T}_k} = 1.13\,\frac{\pi}{2M}\,\left[A^2 - \overline{T}_k^2\right]\,\sigma_\phi \tag{9}$$

Accordingly to the previous equations, if $\hat{T}_k$ is estimated by collecting only one record of M samples in the code histogram, it can be expected that the *Type A uncertainty* is given by

$$u_A(\hat{T}_k) = \sqrt{0.25\,\frac{\pi^2}{M^2}\,\left[A^2 - \overline{T}_k^2\right] + 1.13\,\frac{\pi}{2M}\sqrt{A^2 - \overline{T}_k^2}\;\sigma_{add} + 1.13\,\frac{\pi}{2M}\,\left[A^2 - \overline{T}_k^2\right]\sigma_\phi} \tag{10}$$

The Type A uncertainty for the INL measurements is obviously the same as $u_A(\hat{T}_k)$, while, for the DNL measurements, it is approximately equal to $\sqrt{2}\,u_A(\hat{T}_k)$ [4]. Finally, in order to evaluate the measurement uncertainty, one must combine Type A and Type B uncertainties following the international standards [7].

3 EXPERIMENTAL RESULTS

The experimental results have been obtained with a state-of-the-art test setup. It consists of a low phase noise synthesizer and of a 100MHz crystal oscillator which are phase-locked to the same 10MHz reference signal. The fixed frequency crystal oscillator is AC coupled to an ECL line receiver and then differentially coupled to the ADC clock pins, while the synthesizer is filtered and differentially AC coupled to the ADC input pins. Output data are finally acquired by a high-speed logic state analyzer. The test was performed with an input sinewave of approximately 70 MHz.

After the pass-band filter, the input signal shows a 2nd harmonic below -80dBc and higher-order harmonics more than 10 dB lower. This residual distortion limits the expected Type B uncertainty of the INL measurements for the 12-bit ADC under test to approximatively 0.12 LSB, even if the contribution of the additive noise is made negligible by overdriving. In fact, by (5) it can be argued that the systematic error due to the distortion of the input signal can assume any value between -0.2 LSB and +0.2 LSB and, according to the Guide to the expression of Uncertainty in Measurement, the standard uncertainty of Type B can be estimated as $u_B(INL_k) = 0.2/\sqrt{3}$ LSB.

Since the accuracy in the INL measurement is in any case limited by the spectral purity of the input signal, a reasonable objective seems to be determining the number of samples which are necessary for measuring INL (DNL) with an uncertainty of 0.2 LSB (0.1 LSB, respectively), with a confidence level of the 95%.

Therefore, the systematic effect of the additive noise has to be made negligible by properly overdriving the ADC. Since the standard deviation of the additive noise from both the ADC and the test bench, measured as reported in [9], was approximately $\sigma_{add} = 0.6$ LSB, it has been choosen to overdrive the ADC with a sinewave amplitude of +0.2 dBFS, to ensure that the noise contribution to systematic error is below 0.01 LSB for both the DNL and the INL measurements.

Then, $\Delta\rho/\rho$ has to be considered, for evaluating how much samples have to be acquired. Since in our setup the clock oscillator operates at a fixed frequency, $\Delta\rho/\rho$ is equal to $\Delta f_i/f_i$. From (7) it can be obtained that the number of samples in a single record cannot be higher than

$$M \leq \sqrt{\frac{f_s}{2\Delta f_i}} = 70711 \tag{11}$$

where $\Delta f_i = 0.01$ Hz is the frequency resolution of the input synthesizer and $f_s = 100$ MHz is the clock frequency. This condition is satisfied for instance by $M = 65536$, which represents the memory depth of the logic state analyzer actually in use.

The value of the input frequency can be therefore adjusted so as to meet the quasi-coherent sampling condition by selecting $f_i = 69.99969482$ MHz for having approximately $J = 45875$ periods in a single record. These choices ensure that the equations (7) and (10) can be used.

The phase noise arising from the ADC, the synthesizer and the ECL receiver can be estimated as in [9], or can be evaluated from the data sheets as explained in [8]. Following the second approach, it was found that the standard deviation of the phase noise is approximatively $\sigma_\phi \approx 200\mu$rad.

The predicted variance of the k^{th} element of the INL vector can be now estimated from (10), in the hypothesis that only one record of M samples is acquired to form the histogram. The expected contributions to the Type A uncertainty, which arise respectively from the random initial phase ϕ, the additive noise and the phase noise, are plotted in Fig.2. In the figure the marked line represents the combined effect of these components.

The validity of the equation (10) can be experimentally proved by acquiring $R = 100$ records of $M = 65536$ samples and by estimating R times the INL vector. Fig.3 reports the Type A evaluation of the standard uncertainty of the measured INLs (solid line) and, for comparison, the expected value plotted in Fig.2. Notice that experimental data differ from theoretical ones only for a regular undulatory behaviour which can be ascribed to the particular architecture of the multi-stage ADC under test. In fact, in this architecture, because of the presence of a Track-Hold amplifier in the first stage, it is reasonable that only this stage, apparently a 3-bit ADC, is affected by the phase noise.

Finally, to measure the maximum value of the INL with an expanded uncertainty $U = 0.2$ LSB and a confidence level of 95%, a realistic estimate of the number of records to be acquired is [8]

$$R \geq \max(\sigma^2_{INL_k})\, Z^2_{12,0.95}/(U^2 - 0.33E^2_{INLdist}) \approx 41$$

where $Z_{12,0.95} \approx 4.37$ represents the coverage factor for a confidence level of 95% that not any of the 4095 INL elements will deviate from the measured value by more than $\sqrt{U^2 - 0.33E^2_{INLdist}}$, and $\max(\sigma^2_{INL_k}) = 0.24^2$.

4 CONCLUSIONS

The paper reports the relationships that must be considered in the measurement of INL and DNL for obtaining an a-priori estimate of the expected uncertainty. The results of the presented experiment well agree with the predicted ones, demonstrating the validity of the theory.

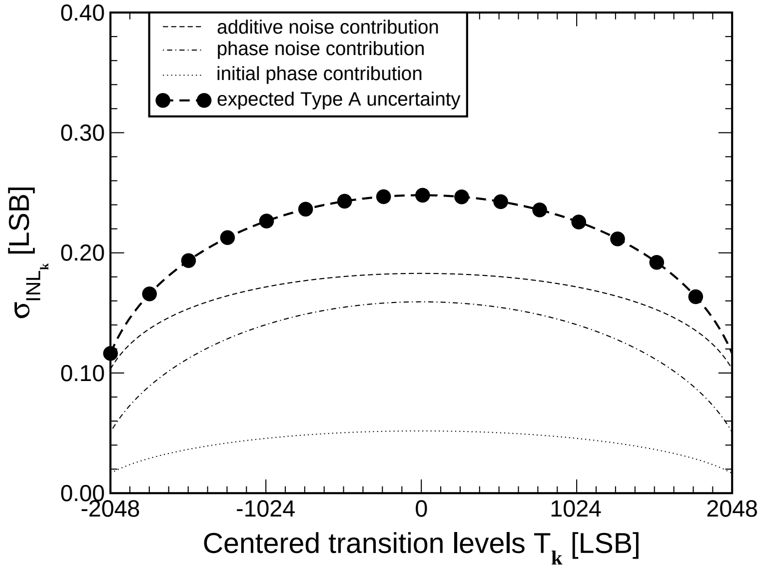

Figure 2: The expected standard deviation of the INL estimates (marked line). Dotted, dashed and dot-dashed lines refer to the contribution of the random initial sampling phase, of the additive noise and of the phase noise, respectively.

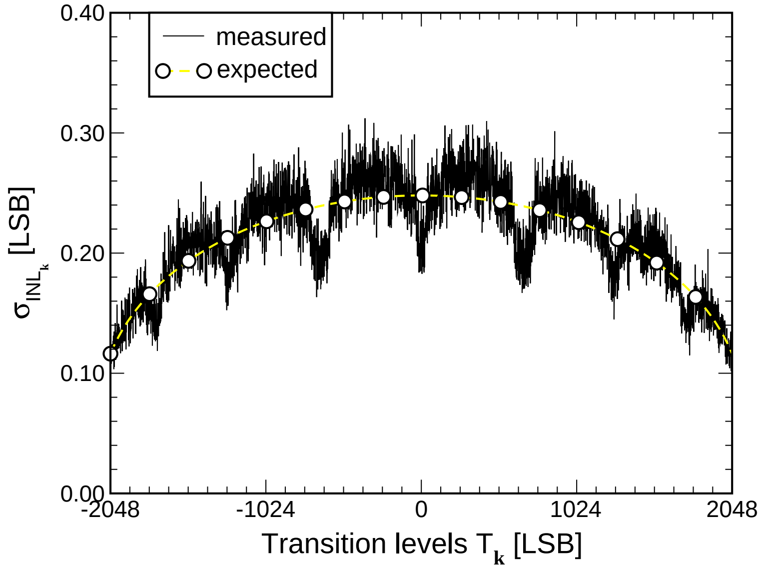

Figure 3: The Type A evaluation of the standard uncertainty of the measured INLs (solid line) compared with the expected one (marked line).

ACKNOWLEDGMENTS

Work supported by the European Commission, SMT programme, project DYNAD, CT-98 2214.

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