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THE 1-1-1-1 CASCADED Σ-Δ MODULATOR

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Abstract: The techniques to design and fabricate a cascaded sigma-delta modulator composed of 4 1^{st}-order sections is presented. By correcting the digital outputs with estimates of the parasitic errors due to analog circuit imperfections, uncancelled quantization noise terms can be removed. Specifically, compensation for the effects of amplifier finite gain and C-ratio mismatches allow for the realization of the 1-1-1-1 cascade. A 1-1-1-1 cascaded modulator, implemented as a fully differential switched-capacitor circuit, has been fabricated in a 1.2μm double-poly n-well CMOS process. Measurements of the modulator verify that for an amplifier gain of 60 dB, and C-Ratio mismatch errors of approximately 0.5%-1%, the error correction offers an overall improvement in SNDR of 12-23 dB. A 12-15 μV_{rms} sine wave can be restored with a positive SNDR for a sampling rate of 2.5 MHz and an OSR of 64.

Key Words: MASH, Cascaded Sigma-Delta Modulator.

1 INTRODUCTION

Cascaded sigma-delta modulators offer an attractive option for high resolution, wide bandwidth A/D conversion. The approach is to cascade several simple sigma-delta modulators, feeding the quantization noise from the preceding stage into the succeeding stage. Quantization noise of the preceding stage is estimated (by the following stage), then it is subsequently subtracted from the output of the preceding stage in the digital post filter.

It is reasonable to expect that idle tones in a cascaded modulator are significantly less than in single stage, higher-order modulators, due to the noise cancellation. However, incomplete cancellation of intermediate noise terms due to matching limitations in standard CMOS processes dramatically increase the sensitivity to finite amplifier open-loop gain and C-Ratio matching errors relative to equivalent single loop modulators. For example, the MASH[1] (1-1-1 cascade) requires an amplifier gain of 85 dB in order to achieve 16-bit performance. In high frequency applications, this is seldom possible since the amplifier gain is often reduced to meet the faster settling requirements. An auto-zeroed integrator[2] can be used to reduce gain sensitivity. However, performance may degrade as higher sample rates are attempted.

Recently attention has been focused on adaptive compensation techniques which remove residual, uncancelled quantization noise due to analog circuit imperfections in cascaded sigma-delta modulators[3–8]. Although cascading can be continued indefinitely, analog circuit imperfections reduce the number of stages in a practical implementation to 2 or 3. Using the techniques described in reference[8], this can be extended to 4 or more stages, within practical limits.

In this paper a compensation scheme which allows for the realization of the 1-1-1-1 cascade shown in figure 1 is presented in section 2. The monolithic integrated circuit, fabricated to verify operation within the audio band, is presented in section 3. The resulting measurements are presented in the final section.

2 COMPENSATION OF 1^{st}-ORDER SECTIONS

A block diagram of the 1-1-1-1 cascaded sigma-delta modulator is shown in figure 1. The noise canceler is divided into two separate blocks: (1) the original noise canceler and (2) a second block which contains a noise canceler to compensate for amplifier gain and matching errors. If we replace the quantizer with an additive noise source, the output stages, Y_1, Y_2, Y_3 and Y_4 can be derived and the system can be characterized.

The original noise cancellation filter, Y_{id} depicted in figure 1, can be expressed in the Z-domain as equation (1) for the 1-1-1-1 network structure:

$$Y_{id1111}(z) = z^{-4}Y_1 + z^{-3}(1-z^{-1})\frac{Y_2}{a} + z^{-2}(1-z^{-1})^2\frac{Y_3}{ab} + (1-z^{-1})^3\frac{Y_4}{abc} \qquad (1)$$

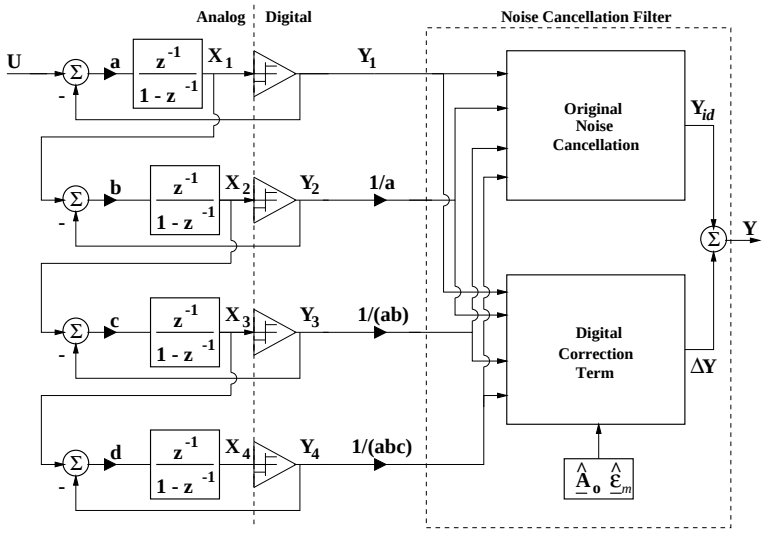

Figure 1. Block diagram of the 1-1-1-1 modulator.

If the model of the integrator includes finite amplifier gain and C-Ratio mismatch, the un-canceled quantization noise [7, 9, 10] from the noise canceler of equation (1) can be expressed as:

$$\begin{aligned}\Delta N(z) \approx\ & z^{-3}[\epsilon_a + (\epsilon_0 - \epsilon_{m1})(1-z^{-1})]N_1 + z^{-2}(1-z^{-1})[\epsilon_b + (\epsilon_0 - \epsilon_{m2})(1-z^{-1})]\frac{N_2}{a} + \\ & z^{-1}(1-z^{-1})^2[\epsilon_c + (\epsilon_0 - \epsilon_{m3})(1-z^{-1})]\frac{N_3}{ab} + (1-z^{-1})^3[\epsilon_d + \epsilon_0(1-z^{-1})]\frac{N_4}{abc} \quad (2)\end{aligned}$$

where $\epsilon_0 = \frac{1}{A_0}$, ϵ_{m1}, ϵ_{m2} and ϵ_{m3} represent the C-ratio mismatch errors and $\epsilon_a = a\epsilon_0$, $\epsilon_b = b\epsilon_0$, $\epsilon_c = c\epsilon_0$, $\epsilon_d = d\epsilon_0$, represent the integrator phase errors of each respective stage.

It has been shown that the un-canceled quantization noise terms can be removed by adding the correction term [8] in equation (3).

$$\begin{aligned}\Delta Y(z) =\ & z^{-2}\left[\epsilon_a + (1-z^{-1})(\epsilon_0 - \epsilon_{m1})\right]\left[\frac{Y_2}{a} - z^{-1}Y_1\right] + \\ & z^{-1}(1-z^{-1})[(\epsilon_a + \epsilon_b) + (1-z^{-1})(2\epsilon_0 - \epsilon_{m1} - \epsilon_{m2})]\left[\frac{Y_3}{b} - z^{-1}Y_2\right]\left(\frac{1}{a}\right) + \\ & (1-z^{-1})^2[(\epsilon_a + \epsilon_b + \epsilon_c) + \\ & (1-z^{-1})(3\epsilon_0 - \epsilon_{m1} - \epsilon_{m2} - \epsilon_{m3})]\left[\frac{Y_4}{c} - z^{-1}Y_3\right]\left(\frac{1}{ab}\right) \quad (3)\end{aligned}$$

This reduces the un-canceled quantization noise to the following expression:

$$\Delta N'(z) \approx (a+b+c+d)\epsilon_0(1-z^{-1})^3\frac{N_4}{abc} \quad (4)$$

The remaining quantization noise level exceeds practical requirements. Equation (3) can be simplified by omitting the final term or the final two terms, without noticeable effects for 18 bit precision.

3 CIRCUIT DESIGN

A monolithic prototype of the 1-1-1-1 cascade, chip 79a, has been fabricated in a 1.2 μm, double-poly, n-well CMOS process. The modulator has been implemented as a fully differential switched-capacitor circuit, depicted in figure 2. There is no dithering.

Chip 79a contains only the modulator portion of figure 1 without the noise canceler. Thus, the quantizer outputs of figure 1, Y_1, Y_2, Y_3 and Y_4 are stored and analyzed in software. This enables us to

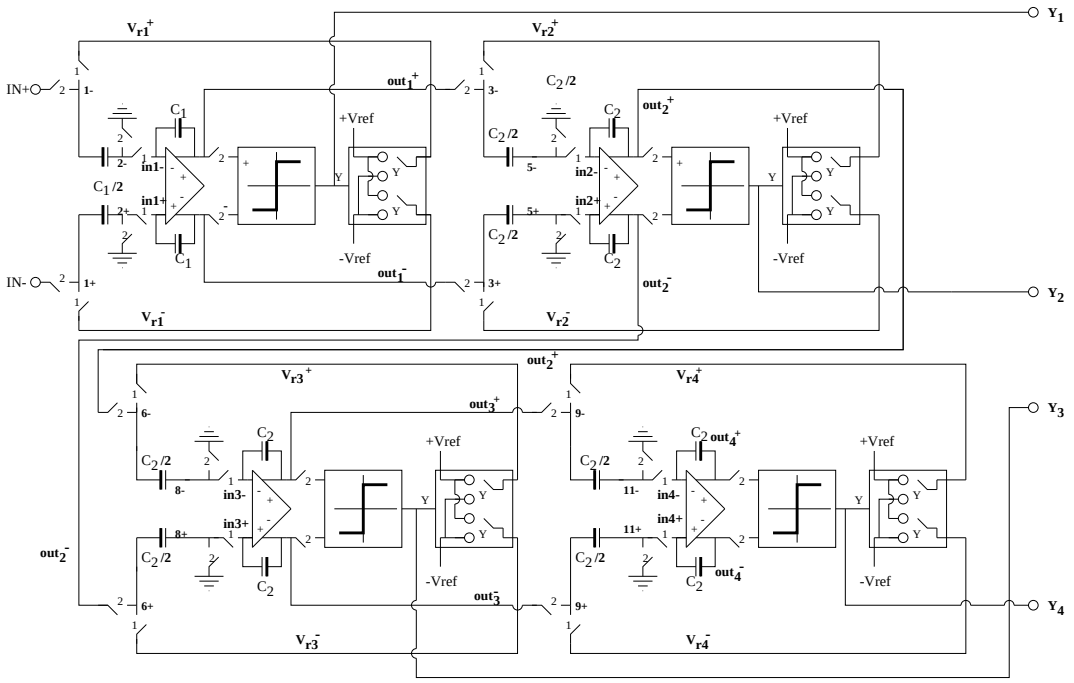

Figure 2. Fully-differential switched-capacitor circuit.

use chip 79a to obtain results for the 1-1, 1-1-1 and 1-1-1-1 cascades as well as a simple, 1^{st}-order Σ-Δ modulator.

The measurement system provides a low distortion input sinusoid, a sample clock with sufficiently low jitter and a frequency stability of 5×10^{-8}. The digital outputs are optically fed to the data memory and then stored on disk. The measurement system used in this work is described in detail in references [11, 12].

Figure 3 shows a micro-photograph of the $2.1mm \times 2.1mm$ chip79a die. The CMOS circuit has been designed for $\pm$2.5V supplies. Both the power and reference voltages are supplied externally and can therefore be varied to suit a wider variety of experimental conditions. The entire 1-1-1-1 modulator occupies a chip area of approximately $0.502mm \times 1.006mm$. $\frac{kT}{C}$ noise is kept to approximately -106 dB for an OSR of 64 using a 2.8 pF input capacitor. All capacitors have been embedded in an n-well connected to analog ground to minimize substrate noise injection from the digital circuitry. Additional copies of the operational amplifiers used in the modulator have been made available with separate connections to estimate the amplifier gain of the integrators in the modulator circuit.

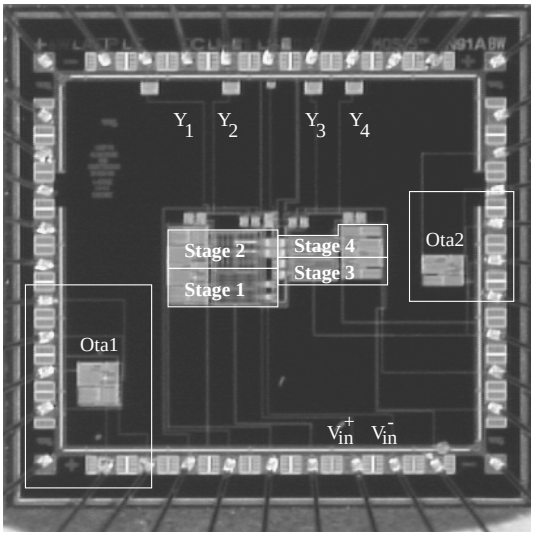

Figure 3. Chip79a die micro-photograph.

The amplifiers have been realized by a fully-differential folded cascode OTA with a passive common-mode feedback circuit. In order to accommodate the large capacitive load of the first stage, the bandwidth

and slew rate of the first amplifier were proportionately increased. The comparators have been realized by a differential input stage followed by a re-settable second gain stage which employs positive feedback to minimize slewing problems. The amplifier swing is limited to slightly less than 1 volt.

4 RESULTS

Estimates of the amplifier gain and C-Ratio mismatch errors provided the parasitic error terms in equation (3). Sample rates of 1 MHz and 2.5 MHz were used to obtain pass band widths of approximately 8 kHz and 20 kHz, respectively. The input signal frequencies were chosen to position the carrier at the same normalized frequency. The frequency of 300 Hz was chosen for the 1 MHz sample rate and 750 Hz, for the 2.5 MHz sample rate.

All spectral analysis was carried out with 2^{19} point FFTs averaged $4X$, using the 7-Term Blackman-Harris Window[13]. Results were amplitude scaled with respect to the comparator reference voltage, V_{ref}, which was set to $\pm$ 1.54 volts. Optimal amplifier gain estimates varied slightly depending upon the input signal amplitude and the sampling rate. At similar amplitudes the optimal gain estimates were very close for both sample rates; however, as the amplitude was increased, the optimal gain estimate dropped. This is most likely due to better agreement with the linear model for moderate input signal amplitudes. The total optimal gain deviation was within $\pm 7.5\%$ in all cases. The optimal C-Ratio mismatch error estimates varied due to changes in the available time for the amplifiers to settle as the sample rate was increased. Equation (3) also compensates for parasitic errors due to linear settling, to a first order approximation.

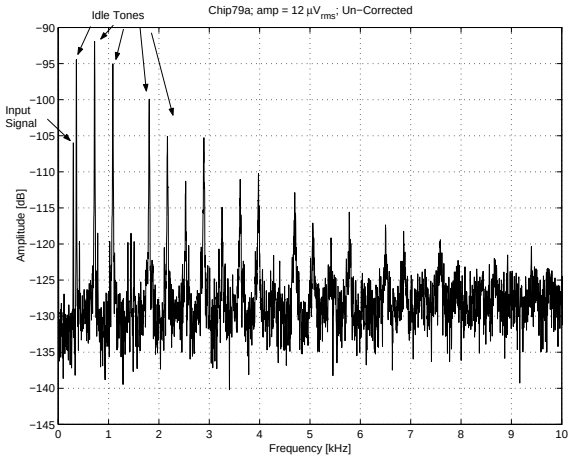

Figure 4. Uncorrected spectrum, $f_s = 1$ MHz.

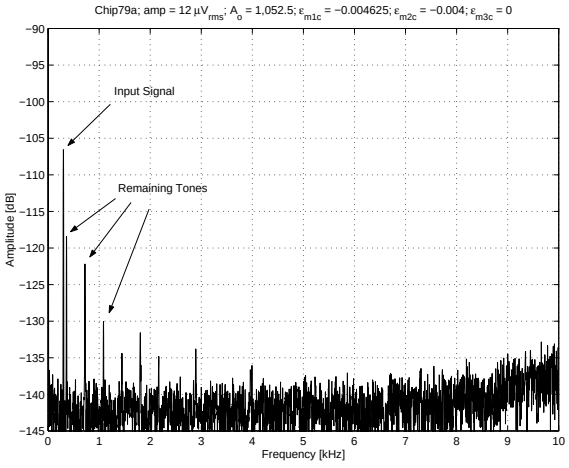

Figure 5. Corrected spectrum, $f_s = 1$ MHz.

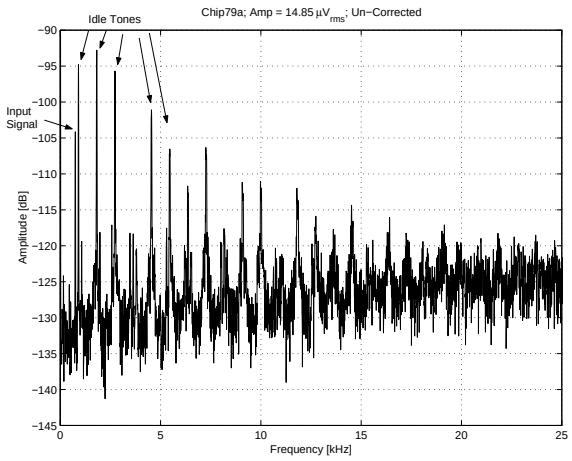

Figure 6. Uncorrected spectrum, $f_s = 2.5$ MHz.

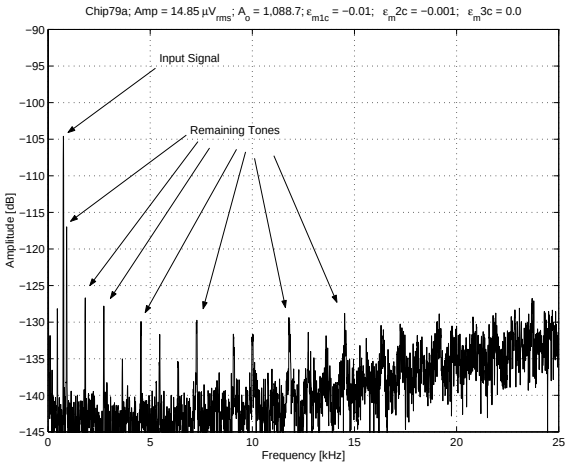

Figure 7. Corrected spectrum, $f_s = 2.5$ MHz.

The spectra presented in figures 4 and 5 were made for measurements taken at a sample rate of 1 MHz and an amplitude of $12\mu V_{rms}$ (-102 dB). The spectra presented in figures 6 and 7 were made for measurements taken at a sample rate of 2.5 MHz and an amplitude of $15\mu V_{rms}$ (-100 dB). This was done to gain a better understanding of how the error correction will work in the presence of settling

errors. In order to see the influence of the amplifier gain estimate, plots of the SNDR vs. the gain estimate, $\hat{\epsilon}_o$, are presented in figures 8 and 9. In each figure, $\hat{\epsilon}_o$ was varied for input signal amplitudes of approximately 12 μV_{rms} (dashed-line) and 300μV_{rms} (solid-line). It can be seen that the 3 dB loss occurs for errors of 10 % or more in all cases with the exception of the 12 μV_{rms} signal at the 1 MHz sample rate. Simulations were carried out using the DelSi[14] tool box, our in-house modeling software,

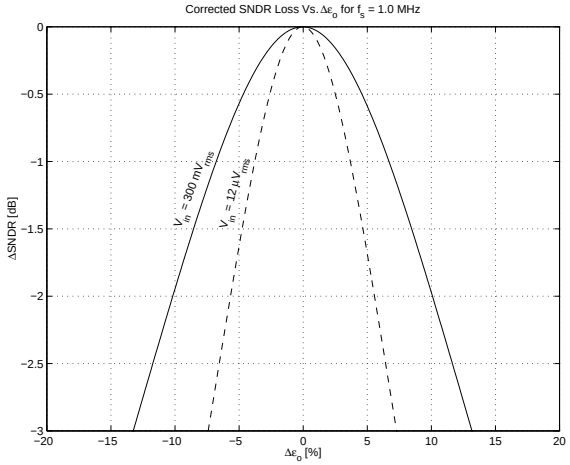

Figure 8. ΔSNDR vs. $\Delta\epsilon_o$ for $f_s = 1.0$ MHz.

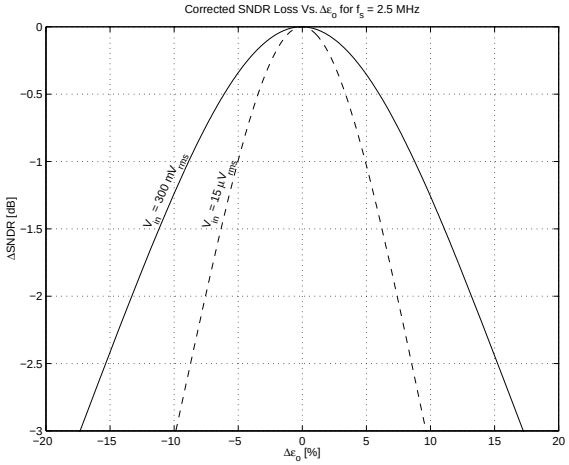

Figure 9. ΔSNDR vs. $\Delta\epsilon_o$ for $f_s = 2.5$ MHz.

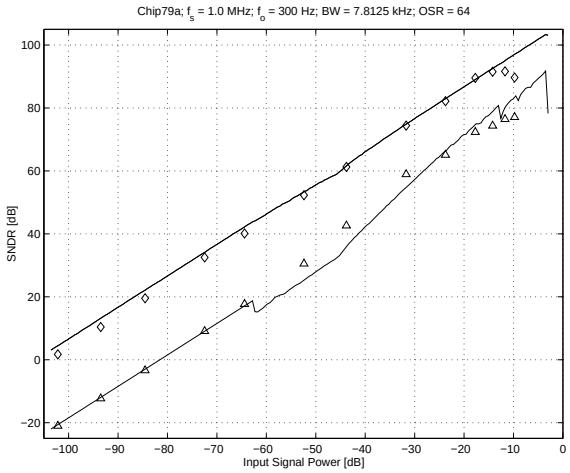

Figure 10. SNDR vs. input signal, f_s=1.0 MHz.

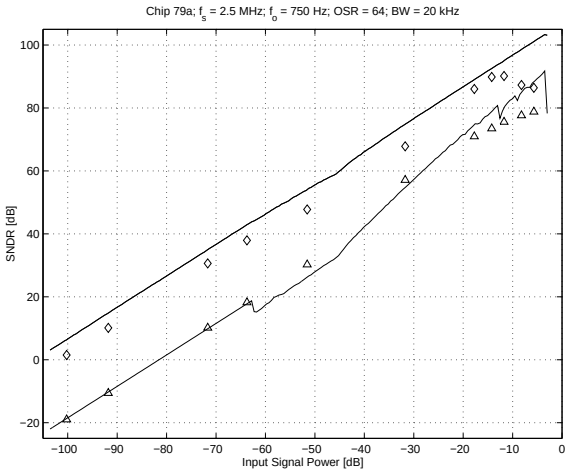

Figure 11. SNDR vs. input signal, f_s=2.5 MHz.

to compare the measurements against expected predictions. The simulations included thermal noise due to the switched-capacitor equivalent resistance of the stage-1 integrator. The simulation results, SNDR vs. input signal power, are displayed in figures 10 and 11 for the 1-1-1-1 cascade at an OSR of 64 for the sample rates of 1 MHz and 2.5 MHz, respectively. The DelSi simulation results are represented by solid lines. Measurements, denoted by the $\diamond$ s and $\triangle$s for the corrected and uncorrected outputs were superimposed over the simulated curves.

The SNDR degrades for input signals above -15 dB in figures 10 and 11. This is due to limitations in the swing and linearity of the amplifier; however, for the 2.5 MHz sample rate this is also limited by the finite settling of the amplifiers.

5 SUMMARY

By removing the residual, uncanceled 1^{st} and 2^{nd} order quantization noise terms, the realization of a 4-stage cascaded modulator was demonstrated for an OSR of 64. Digital correction must be employed for reliable operation. With estimates of the amplifier gain and the C-Ratio mismatch between stages 1 and 2, digital correction will yield 12-23 dB improvement in SNDR making 18-20 bit performance achievable with practical sample rates using cascades of 1^{st}-order modulators. Using this technique, the performance is limited the $\frac{kT}{C}$ noise and the linearity of the stage 1 amplifier over the desired swing range. The amplifier gain estimate can vary by as much as $\pm$10% without severely degrading the spectral resolution in most cases.

The most critical parameters are the amplifier gain estimate and the C-Ratio mismatch error between stages 1 and 2. The amplifier gains were well matched, but they were not exact. From this work we found that separate estimates of the amplifier gain for stages 1, 2 and 3, resulted in a negligible improvement (0.1 dB). Thus, a single amplifier gain estimate seems to be adequate. While knowledge of the amplifier gain is helpful, equation (3) can also correct for other types circuit imperfections as long as the parasitic terms are accurately represented by equation (2). Thus, errors due to linear settling and offset can also be corrected.

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