

FLEXIBLE ADC: A DITHER AND OVERSAMPLING BASED SOLUTION TO IMPROVE THE PERFORMANCE OF ADC SYSTEMS

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Abstract: A well-known technique that can be used to increase the resolution of ADC digitising systems is based on dithering, oversampling and noise shaping. Dithering assures a uniform power spectral density for the quantisation error, oversampling. Followed by digital filtering, it improves signal to noise ratio and effective number of bits at the expenses of the input signal bandwidth. Noise shaping removes quantisation error power from signal bandwidth. The present paper introduces the concept of a flexible ADC that can be applied to an ordinary data acquisition board as a solution to optimise digitising systems performance for different sampling rates. Gains of ten or more effective bits can be obtained, for low frequency input signals, using always the maximum sampling rate of the ADC together with dithering, oversampling and noise shaping techniques.

Keywords: Dither, Oversampling, Noise Shaping.

1 INTRODUCTION

Two main performance parameters in any digitising system are resolution and sampling rate. Unfortunately, sampling rate and resolution are usually competing interests in the design of any acquisition system, but for a single ADC system substantial gains in resolution can be obtained for input signals with low bandwidth compared with ADC sampling rate.

In the present paper, dithering and noise shaping techniques are used together with oversampling to optimise the performance of an ADC based digitising system. Two different hardware configurations are considered to obtain a flexible ADC implementation: one based on a combination of an ADC and a digital signal processor (DSP) and another one based on an ordinary data acquisition board (DAQ) with external trigger and clock capabilities. In both configurations, the ADC is used in oversampling mode with a sampling rate equal to its maximum value. The overall digitising system behaves, from the view point of topology, as a multibit sigma-delta (Σ - Δ) converter, which takes advantages of digital signal processing techniques to increment output signal-to-noise relation at the expenses of input signal bandwidth. Effective sampling rate of the output digitised signal is much lower than ADC sampling rate due to the usage of decimation, but its resolution varies inversely with the input signal bandwidth.

Section 2 gives an overview of the basic concepts related to dithering, oversampling and noise shaping, highlighting the compromise between resolution and bandwidth for an oversampled ADC system, and introducing two different hardware solutions to implement the flexible ADC. Simulated and experimental results are presented in sections 3.1 and 3.2, respectively. Section 4 is dedicated to conclusions and future developments.

2 SYSTEM DESCRIPTION

Figure 1 represents two possible solutions for the hardware block diagram of a flexible ADC. One of the solutions (Figure 1(a)) is based on a DAQ board connected to a personal computer (PC) that performs filtering and decimation functions. Optional synchronisation between signal triggering and sampling can be provided by a phase locked loop (PLL) used as a frequency multiplier with a factor equal to the oversampling factor (N). In this case, external triggering and clock capabilities of DAQ board must be available. Another solution, represented in Figure 1(b), is based on a DSP whose fast on-chip, fixed or floating point, multiplier allows the device to perform fundamental digital signal processing operations, such as filtering and decimation, with optimum efficiency.

Figure 2 represents the connections between the noise shaper block diagram and the flexible ADC. Noise shaping can be used to obtain additional reduction of quantisation error inside the signal bandwidth. The first order modulator, associated with the ADC, shapes the quantisation error power

density so that it lies above the passband of the digital output filter. The effective number of bits (ENOB) that can be reached is therefor much larger than would otherwise be expected from the oversampling ratio without noise shaping.

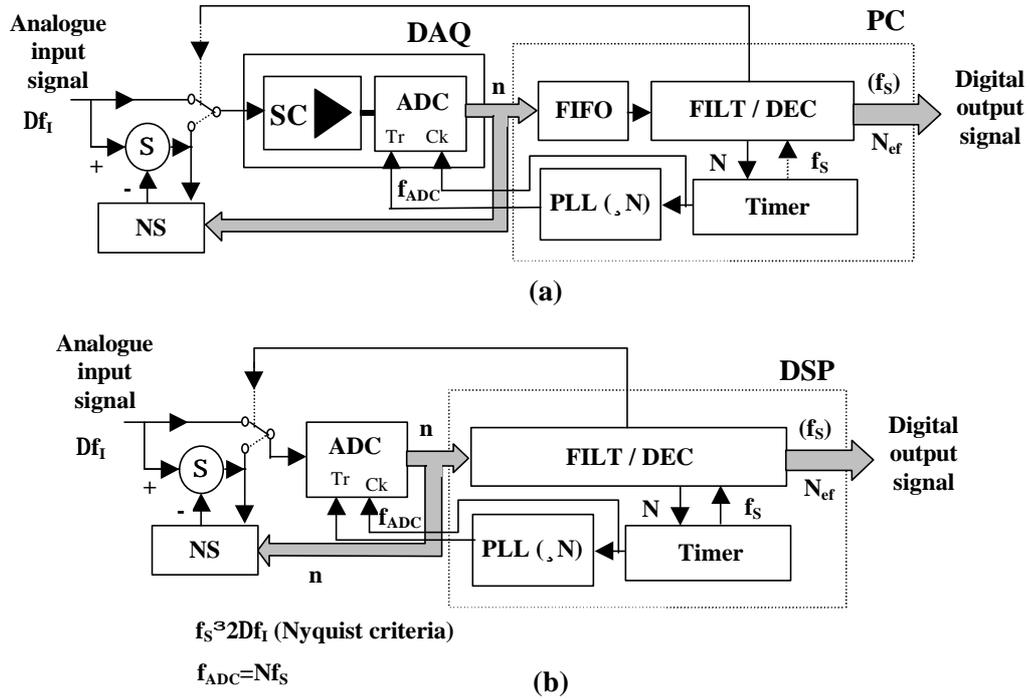


Figure 1. Hardware block diagram of a flexible ADC: (a) using a data acquisition board and a PC; (b) using an ADC and a DSP (PC- personal computer; SC- signal conditioning circuits; PLL- phase locked loop; FILT- filtering; NS- noise shaping; DEC- decimation; FIFO- first-in first-out memory; Tr- trigger input; f_{ADC} - ADC sampling rate; Δf_i - input signal bandwidth; f_s - effective sampling rate; N- oversampling factor).

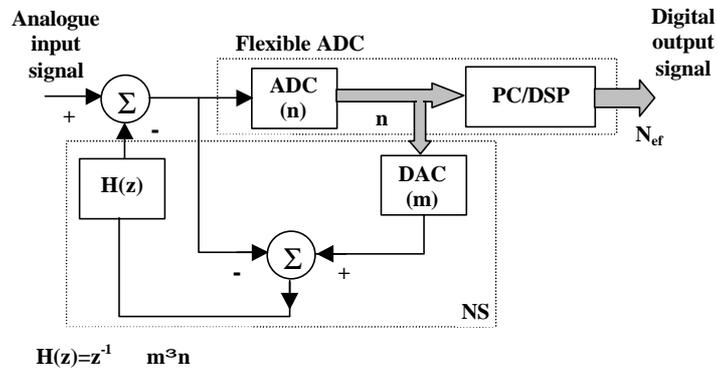


Figure 2. Connections between the noise shaper block diagram and the flexible ADC (NS- noise shaper; n- number of bits of the ADC; m- number of bits of the DAC).

2.1 Oversampling, filtering and dithering

The ADC sampling rate (f_{ADC}) is equal to its maximum value and the effective sampling rate (f_s), taken from the PC or DSP, depends on the input signal bandwidth (Δf_i). The effective number of bits (N_{ef}) obtained after digital filtering varies in a logarithmic way with the oversampling factor (N) [1]:

$$N_{ef} = n + \frac{1}{2} \log_2 \left(\frac{N}{1 + k^2} \right) \quad (1)$$

where n represents the number of bits of the ADC, k the normalised dither amplitude referred to the ADC quantisation step (Q), and the oversampling factor (N) is defined by the ratio between ADC sampling rate and Nyquist rate (f_N) of the input signal, defined by:

$$f_N = 2\Delta f_i \quad (2)$$

where (Δf_i) represents the input signal bandwidth.

From (1) we conclude that for each additional effective bit we must increment the oversampling by a factor equal to four. Consequently, the relation between input signal bandwidth (Δf_i) and ADC sampling rate (f_{ADC}) is given by the following expression:

$$\frac{\Delta f_i}{f_{ADC}} = \frac{\Delta f_i}{Nf_s} = \frac{1}{2(1+k^2)2^{2(N_{ef}-n)}} \quad (3)$$

From the last expression we obtain the well known result that the input signal bandwidth is reduced to one quarter of its value for each additional effective bit gain when oversampling and filtering techniques are used.

In order to assure a uniform power spectral density of the quantisation error [2], self-dithering provided by the noise naturally added to the signal and by the ADC internal noise is usually enough, considering that the amplitudes of those noise signals are adequate for dithering purposes. These noise signals are also assumed to be uncorrelated with the analogue input signal of the converter. If this is not the case, or if large-scale dithering is required to minimise ADC non-linearities [3], an additive or subtractive topology must be considered (Figure 3), and for the last case expressions (1) and (2) are still valid with $k=0$. For deterministic dithering with an auto-subtractive topology, dither subtraction is achieved without the need of an actual subtractor. The subtracting effect is maintained as long as the dither experienced by the input signal exhibits a zero mean value and the linear filter averages the digital output signal over an integer number of dither periods.

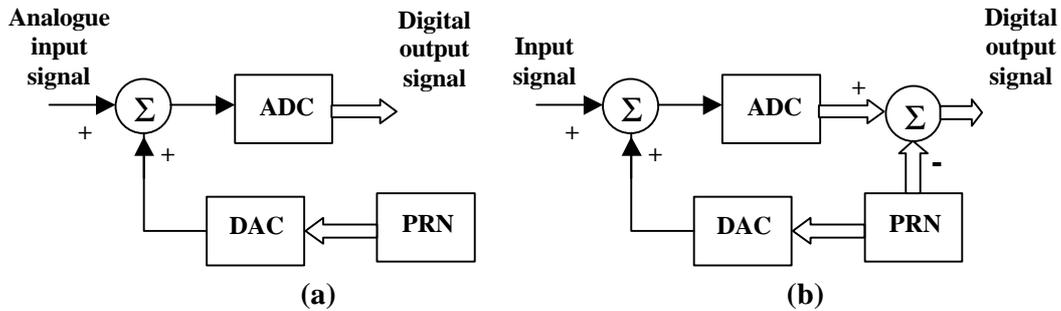


Figure 3. Dither insertion topologies: (a) additive or auto-subtractive; (b) subtractive (PRN- pseudo random noise).

2.2 Noise shaping

Additional gains in effective number of bits, without so high bandwidth penalties, can be obtained with the usage of noise shaping techniques that remove quantisation error from signal bandwidth (base-band) to out-of-band, and is afterwards cancelled by filtering.

Supposing that the quantisation error density is frequency independent in the band $f=0$ to $f=f_{ADC}/2$, the total noise power associated with the quantisation error for a first-order noise shaper (Fig. 2), after filtering, is given by [4]:

$$N_Q = \int_0^{f_s/2} n_q^2 \left| 1 - e^{-j2\delta f/f_s} \right|^2 df \quad (4)$$

where n_q^2 represents the power density of uniform quantisation error. Using Euler's relationship and some trigonometric equalities, the result of the integration represented by (4) is equal to:

$$N_Q = 4 \frac{Q^2}{12} \left[\frac{1}{2N} - \frac{1}{2\delta} \sin\left(\frac{\delta}{N}\right) \right] \quad (5)$$

where Q represents the quantisation step of the ADC and N the oversampling factor previously defined.

The signal-to-noise relation gain (SNR_G) associated with filtering and noise shaping is given by:

$$SNR_G = \frac{Q^2/12}{N_Q} = \frac{1}{4} \left[\frac{1}{2N} - \frac{1}{2\delta} \sin\left(\frac{\delta}{N}\right) \right]^{-1} \quad (6)$$

Using a third order Taylor series approximation for the function $\sin(x)$:

$$\sin(x) \cong x - \frac{x^3}{6} \tag{7}$$

it is possible to obtain:

$$\text{SNR}_G = \frac{1}{4} \left[\frac{1}{2N} - \frac{1}{2} \left(\frac{p}{N} - \frac{p^3}{6N} \right) \right]^{-1} = \frac{3N^3}{\delta} \tag{8}$$

and using logarithmic units:

$$\text{SNR}_G(\text{dB}) \cong 30\log_{10}(N) - 5.2 \text{ dB} \tag{9}$$

From the last expression it is possible to confirm that for each duplication of the oversampling factor ($\Delta N=2$), the signal to noise relation gain (ΔSNR_G) is equal to 9 dB, which corresponds to a gain of 1.5 effective bits of the digitising system. This means that for the same oversampling factor ($N \gg 1$), the effective number of bits gain with noise shaping is three times higher than the one obtained with oversampling and filtering alone.

3 RESULTS EVALUATION

A LabVIEW simulator was developed to study global effects of oversampling, dithering and noise shaping techniques on signal digitalisation.

Experimental results to confirm the effective number of bits gain as a function of the input signal frequency were obtained with a Keithley-Metrabyte data acquisition board (DAS4102) that has the following main characteristics: maximum sampling rate=64 MS/s; ADC number of bits: n=8 (flash type); ADC internal sampling rates: 0.5; 1.0; 2.0; 4.0; 8.0; 16.0; 32.0; 64.0 MS/s.

3.1 Simulation results

The main input parameters of the simulator are: oversampling factor (N), signal and noise amplitudes, dither characteristics – amplitude, period and type, number of bits (n) of the ADC, digitalisation options – filtering, decimation and noise shaping and sine wave curve fitting convergence parameters – maximum number of iterations and tolerance (maximum error).

The main output parameters of the simulator are: sine wave interpolated signal, conversion error and effective number of bits of the digitised output signal. The four parameters (amplitude, frequency, initial phase and offset) least mean squares algorithm for sine wave fitting [5], using matrix operations, was fully implemented in LabVIEW. Non-linearity errors of the converter can also be easily added to the ADC model virtual instrument (VI).

Figure 4 represents the front panel of the virtual instrument and in Figure 5 are presented simulator results for an oversampling factor (N) between 2^4 and 2^{16} , a six bit ADC (n=6) and a uniform dither component with the following characteristics: amplitude equal to 1 LSB (least significant bit) and period equal to 16.

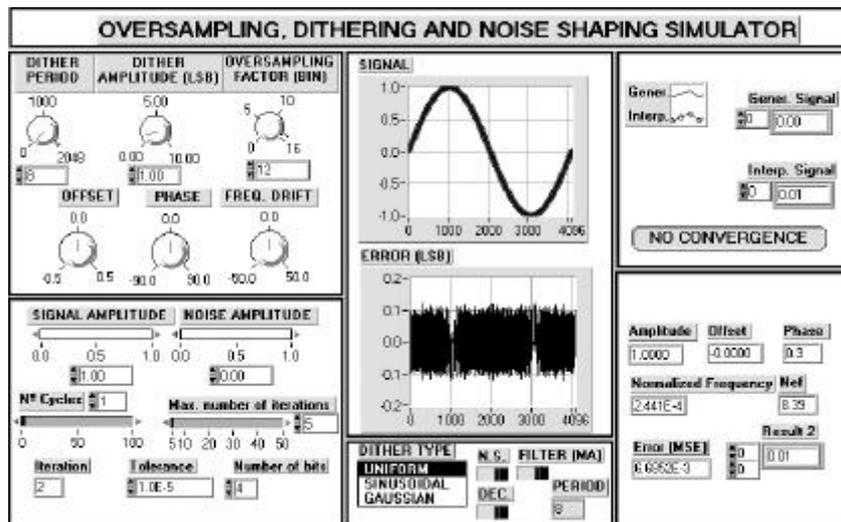


Figure 4. Front panel of the LabVIEW virtual instrument used for simulation.

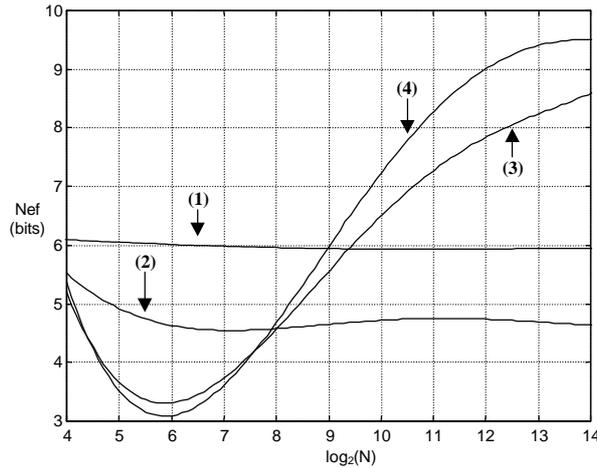


Figure 5. Simulated results: (1)- without dither, filtering and noise shaping; (2)- with dither, noise shaping and no filtering; (3)- with dither, filtering and no noise shaping; (4)- with dither, filtering and noise shaping.

As main conclusions after several simulations it is important to refer that filtering and noise shaping techniques require a minimum value of oversampling factor in order to be effective (signal amplitude variation between samples less than 1 LSB); noise shaping advantage over filtering is only visible when the oversampling factor is larger than a minimum value (in the example $N=2^8$). For each oversampling factor value there is a optimal value of dither period and amplitude that maximises digitising system performance.

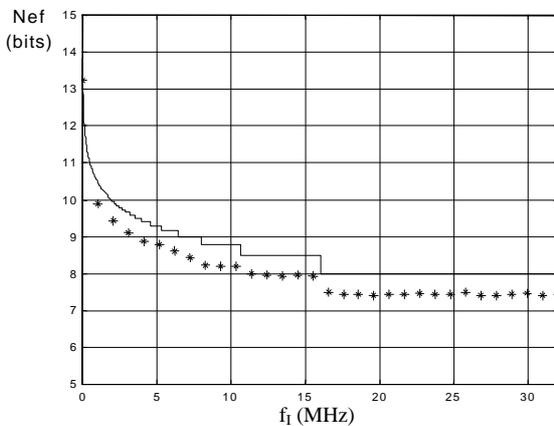
3.2 Experimental results

Experimental results, represented in Figure 6, were obtained using a DAQ board from Keittley-Metrabyte (DAS4102) and a sine wave generator with enough accuracy for an eight-bit converter (HP33120-A).

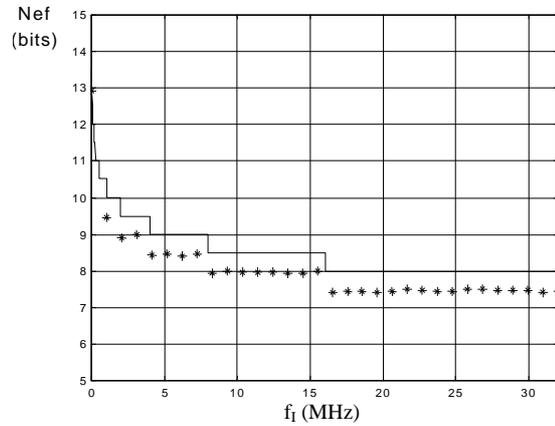
Curve (a) represents the effective number of bits (ENOB) as a function of input signal frequency, assuming a maximum integer oversampling factor without application of noise shaping techniques. Curve (b) represents the same kind of data for an oversampling factor equal to an integer power of two. Finally curve (c) represents the effective number of bits (ENOB) as a function of input signal frequency, assuming a maximum integer oversampling factor equal to an integer power of two but with application of noise shaping techniques.

Effective number of bits evaluation was based on the sine wave curve fitting algorithm (four parameters). Synchronisation between the external clock and triggering of the data acquisition board was provided by a phase locked loop (PLL) circuit.

These results clearly show the advantages that can be obtained with the proposed method, especially when low frequency signals are present at the input of the digitising system.



(a)



(b)

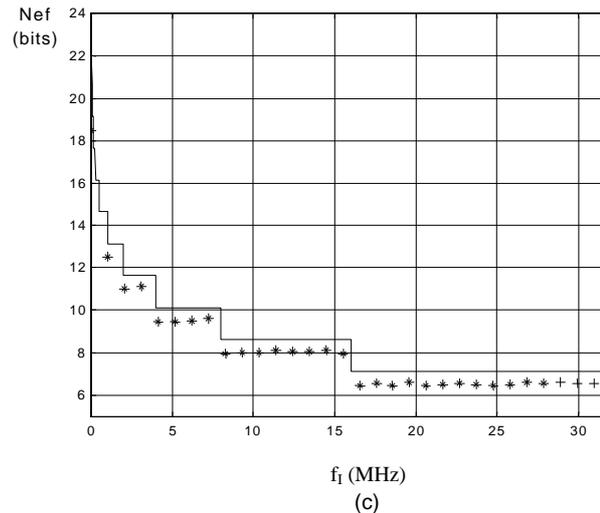


Figure 6. Effective number of bits as a function of input signal frequency for an 8 bit converter: (a) maximum integer oversampling factor without noise shaping; (b) maximum integer power of two oversampling factor without noise shaping; (c) maximum integer power of two oversampling factor with noise shaping (continuous line – theoretical results; symbol ‘*’ – experimental results).

Maximum relative difference between experimental and expected theoretical effective number of bits is lower than 5%. This difference can be explained taking into consideration the differential non-linearity (DNL) and integral non-linearity (INL) errors of the DAQ board which are equal to 0.6 LSB, its maximum signal-to-noise relation equal to 46.3 dB ($N_{ef}=7.4$), distortion of input signal generator and other errors associated with digital signal processing, like coefficient quantisation and truncation errors of digital filters.

4 CONCLUSIONS AND FUTURE DEVELOPMENTS

Simulated and experimental results show clearly the advantages of the proposed principle of the flexible ADC. The technique can be applied to an ordinary DAQ board and assures a complete usage of ADC performance for all effective sampling rates. Gain of 1.5 bits can be obtained for each doubling of oversampling factor (N). At the same time, usage of oversampling minimises the accuracy requirements of the sample-and-hold amplifiers, eases the design of antialiasing filters and minimises differential non-linearity errors (DNL) that are a serious problem for low amplitude signals [6].

Results obtained with the simulator, developed to study global effects of dithering, noise shaping, filtering and decimation, in the presence of input non-stationary signals, point out that for deterministic dither there is an optimum value of dither amplitude and period for each value of oversampling factor.

As future developments of the present work, it will be considered an automatic selection of the oversampling factor based on the input signal frequency contents obtained using a FFT algorithm. This capability, together with the flexible ADC concept introduced in this paper, creates what we can call “smart ADC” with an automatic selection of resolution as a function of the input signal bandwidth.

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