**XVI IMEKO World Congress**
Measurement - Supports Science - Improves Technology - Protects Environment ... and Provides Employment - Now and in the Future
Vienna, AUSTRIA, 2000, September 25-28

# EXPERIMENTAL VERIFICATION OF A NEW METHOD FOR EFFECTIVE RESOLUTION EVALUATION

***Konrad Hejn, Jerzy Jędrachowicz and Antoni Leśniewski***
Institute of Electronic Systems
Warsaw University of Technology
ul. Nowowiejska 15/19, 00-665 Warsaw, Poland

*Abstract: The paper presents experimental results obtained with three methods of effective resolution evaluation. We compare the measurement repeatability of the traditional method specified by* IEEE *standard with the repeatability of the* two-point *heuristic method developed and published two years ago and that of a* new *analytic method developed recently. Verification of measurements was carried out using standard video-frequency-band ADCs.*

*Keywords:Analog-digital conversion, Effective resolution, Error analysis, IEEE standards, Mixed-signal testing, Quantization.*

## 1. INTRODUCTION

The practical significance of the effective resolution (efr) is that the quality of a non-ideal Analog to Digital Converter (ADC) can be made measurable. One can objectively select the most applicable converter by the comparison of numerical data. To measure the efr it is first necessary to choose a test signal $\boldsymbol{u}$. The test signal is then applied to the input of ADC under test and the quantized output $\{y(m),\ m = 1,\ldots,M\}$ is recorded. The discrete-time quantization error $\boldsymbol{e}$ is defined in Widrow's model [1] as a random difference between quantized output and the input test signal, Fig.1

$$\boldsymbol{e} = \{\boldsymbol{e}(m) = \boldsymbol{y}(m) - \boldsymbol{u}(m),\ m = 1,\ldots,M\} \tag{1}$$

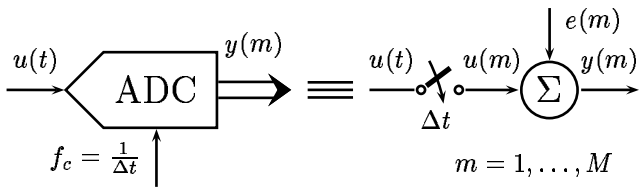


Figure 1. A discrete-time model of an ADC under test.

A 'large' pure sine wave of a stable frequency $f_0$

$$\boldsymbol{u}(m) = V\cos(Fm + \boldsymbol{P}) + C,\ m = 1,\ldots,M \tag{2}$$

is usually recommended as an appropriate test signal. The digital frequency $F$ is defined as $F = 2\pi f_0\,\Delta t$, where $\Delta t$ is the sampling period. The DC offset $C$ and the amplitude $V$ are stable during the experiment but known only approximately. While the initial phase $\boldsymbol{P}$ is usually not known, it can be theoretically modeled by a random variable with a uniform distribution in the range $(-\pi, \pi)$ [2].

In practice, only the digitized record (and not the original analog signal) is available for analysis. Hence, after extracting the signal's parameters from the recorded data, we substitute the same initial phase for the input and output signals. Consequently, to measure the ADC quality one may compare the theoretical ("reference") standard deviation $\sigma_0$ of the quantization error with its measured estimate $s_0$, namely

$$\text{efr} \stackrel{\text{def}}{=} R\,\frac{\sigma_0}{s_0} \tag{3}$$

where $R$ denotes the nominal resolution of the ADC under test. The main difficulty is how to determine both $\sigma_0$ and $s_0$ used in the definition (3).

The well known weakness of the IEEE method [3, 4] results from the assumption that the quantization error has a uniform distribution. The IEEE method leads in general to biased efr estimates. The bias can be so significant, that the measurement repeatability might not be acceptable — especially, when a real converter appears to be better than the perfect one! To illustrate the problems of the *IEEE* (that is traditional) method and the strength of the proposed *two newer* (that is heuristic and analytic) methods, we evaluated the efr from the same records captured.

## 2. FORMULAS NEEDED

The detailed theory of the *new analytic* method is presented in [5]. Here we quote only the formulas used by the verification algorithm. Assuming the perfect ADC and test signal (2) we have the following four formulas for the average value $\overline{y}$ and the average square value $\overline{y^2}$ (sample means) of the digital output $\boldsymbol{y}$ and for the mean value $\mathcal{E}\boldsymbol{e}$ and the mean-squared value $\mathcal{E}\boldsymbol{e}^2$ (expectation means) of the quantization error $\boldsymbol{e}$ respectively

$$\overline{y} = \frac{K_0 + K_1}{2} - \frac{1}{\pi} \sum_{k=K_0+1}^{K_1} \arcsin \beta_k \tag{4}$$

$$\overline{y^2} = \frac{K_0^2 + K_1^2}{2} - \frac{2}{\pi} \sum_{k=K_0+1}^{K_1} (k - \frac{1}{2}) \arcsin \beta_k \tag{5}$$

and

$$\mathcal{E}\boldsymbol{e} = -C + \frac{K_0 + K_1}{2} - \frac{1}{\pi} \sum_{k=K_0+1}^{K_1} \arcsin \beta_k \tag{6}$$

$$\mathcal{E}\boldsymbol{e}^2 = \frac{V^2}{2} + \frac{(C-K_0)^2}{2} + \frac{(C-K_1)^2}{2} - \frac{2V}{\pi} \sum_{k=K_0+1}^{K_1} \left( \beta_k \arcsin \beta_k + \sqrt{1-\beta_k^2} \right) \tag{7}$$

where

$$K_0 = \text{floor}\left(C + \frac{1}{2} - V\right) \quad K_1 = \text{floor}\left(C + \frac{1}{2} + V\right) \quad \beta_k = \frac{1}{V}(k - \frac{1}{2} - C) \tag{8}$$

and floor represents rounding down to the nearest integer. Equations (4), (5), (6), and (7) are implicitly dependent on $C$ and $V$, since $K_0$, $K_1$, and $\beta_k$ depend on $C$ and $V$.

The right-hand sides of equations (4) and (6) differ (in conformity with expectation) by DC offset $C$.

The above formulas lead to a *new* (improved) definition of the efr [6], namely

$$\text{efr}_{new} = \frac{R\,\sigma_{\boldsymbol{e}}(\widehat{C},\widehat{V})}{\sqrt{\overline{\widehat{e}^2} - \left(\overline{\widehat{e}}\right)^2}} \overset{\text{IEEE}}{\underset{\text{simplification}}{\Longrightarrow}} \frac{R}{\sqrt{12\,\overline{\widehat{e}^2}}} = \text{efr}_{IEEE} \tag{9}$$

where $\widehat{C}$ and $\widehat{V}$ are estimated from captured digital data as a solution of equations (4) and (5). The numerator is evaluated from formulas (6, 7) but the denominator again from captured digital data.

In contrast, the IEEE standard uses the straightforward formulas for the estimates

$$\widehat{C}_{IEEE} = \overline{y} \tag{10}$$

$$\widehat{V}_{IEEE} = \sqrt{2(\overline{y^2} - \overline{y}^2)} \tag{11}$$

They follow from the incorrect assumption that the DC offset $C$ and amplitude $V$ are exactly the same on both the analog input and digital output of the tested ADC. The heuristic *two-point* method [7] has partly corrected this incorrect simplification. It applies two data records $y_1$ and $y_2$ instead of one and uses slightly improved estimates

$$\widehat{C}_{two-point} = \frac{1}{2}\left(\overline{y_2} - \frac{1}{2} + \overline{y_1}\right) \tag{12}$$

$$\widehat{V}_{two-point} = \frac{\sqrt{2(\overline{y_2^2} - \overline{y_2}^2)} + \sqrt{2(\overline{y_1^2} - \overline{y_1}^2)}}{2} \tag{13}$$

## 3. VERIFICATION PROCEDURE

The flow diagram of our verification procedure is shown in Fig.2. It comprises a comparison between the traditional *IEEE* method (the left path) and the *new analytic* method (the right path). To keep the flowchart legible, the blocks representing the *two-point* method are not shown.

Note that there are more than two (that is the left and right) paths. This fact can be a possible reason why the results obtained from the same data record by different researches are not repeatable. Another reason is that instead of using the formulas (6) and (7) one can obtain the mean value $\mathcal{E}e$ and the mean-squared value $\mathcal{E}e^2$ by simulation. It takes time but for sufficiently long records $\mathcal{E}e = \overline{e}$ and $\mathcal{E}e^2 = \overline{e^2}$. We fixed the record length for $M = 32$ Ksamples in all our experiments, that have exhibited sufficient accuracy for converters of up to 8 bits.

Since our main aim was to investigate the repeatability of all the three methods the values of stimulus parameters $C$ and $V$ (2) have been intentionally modified with a random number generator and they were also uncontrollably modified by the thermal processes in the ADC. Each presented histogram is a result of the analysis of 1000 records which were captured for randomly fixed couples of $(C, V)$. It means that the flow diagram from Fig.2 is always executed 1000 times to obtain one histogram.

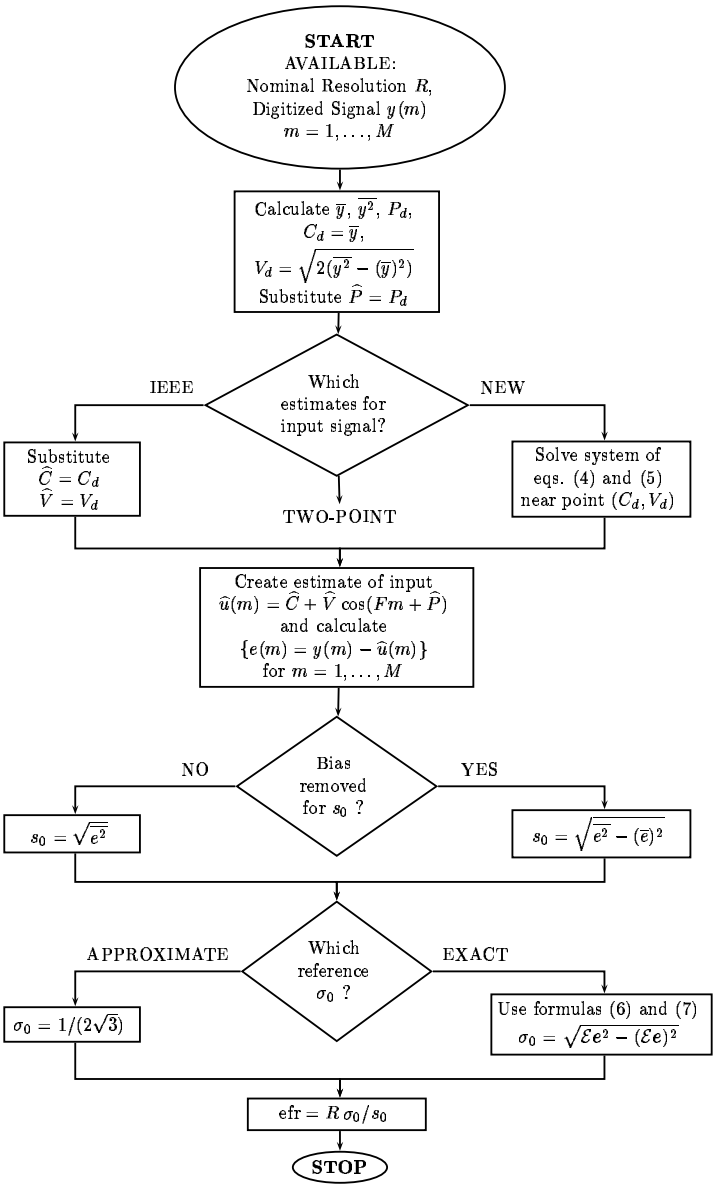


Figure 2. The flowchart of the verification algorithm.

## 4. MEASUREMENT SETUP

The setup of all our experiments is shown in Fig.3. It integrates the hardware-software environment of MXI/VXI–C/SCPI/VEE [8, 9] that has enabled the design of a tester required for the experimental verification of the discussed methods.

The tested ADC is connected to the tester with a carefully designed *fixture*. This circuitry is a part of the precise mixed-signal interface between the tester and the ADC. It includes, among others, a selective analog filter and a finite state machine implemented in an FPGA.

The necessary *hardware* that is responsible for metrological and/or operational parameters of the tester consists of the following major components: VXI Subsystem Mainframe (HP E1401A), slot0 MXI/VXI Interface (HP E1482B), 160 MHz Timing Module (HP E1450A), 20 MHz Pattern IO modules (HP E1451A and E1452A), active Timing and Pattern Pods with cables (HP E1453A and HP E1454A), 21 MHz Synthesized Function/Sweep Generator (HP E1440A), Summing Amplifier/DAC (HP E1446A), and Power Supply (HP E3631A). The system allows sampling rates of up to 5 MHz (minimum sampling period $\Delta t = 200$ ns). The sampling period used in all the histograms presented in this paper is 2 $\mu$s.

Both the application software and its installation platform played a vital role in the design of the tester. The controller (an external workstation Model 715 with the MXI bus interface) communicates with an embedded VXI bus extender on the register transfer level. It means that the communication is fast. The C/SCPI preprocessor is a software tool which supports the programming of the register-based modules using the SCPI command set [10, 11].

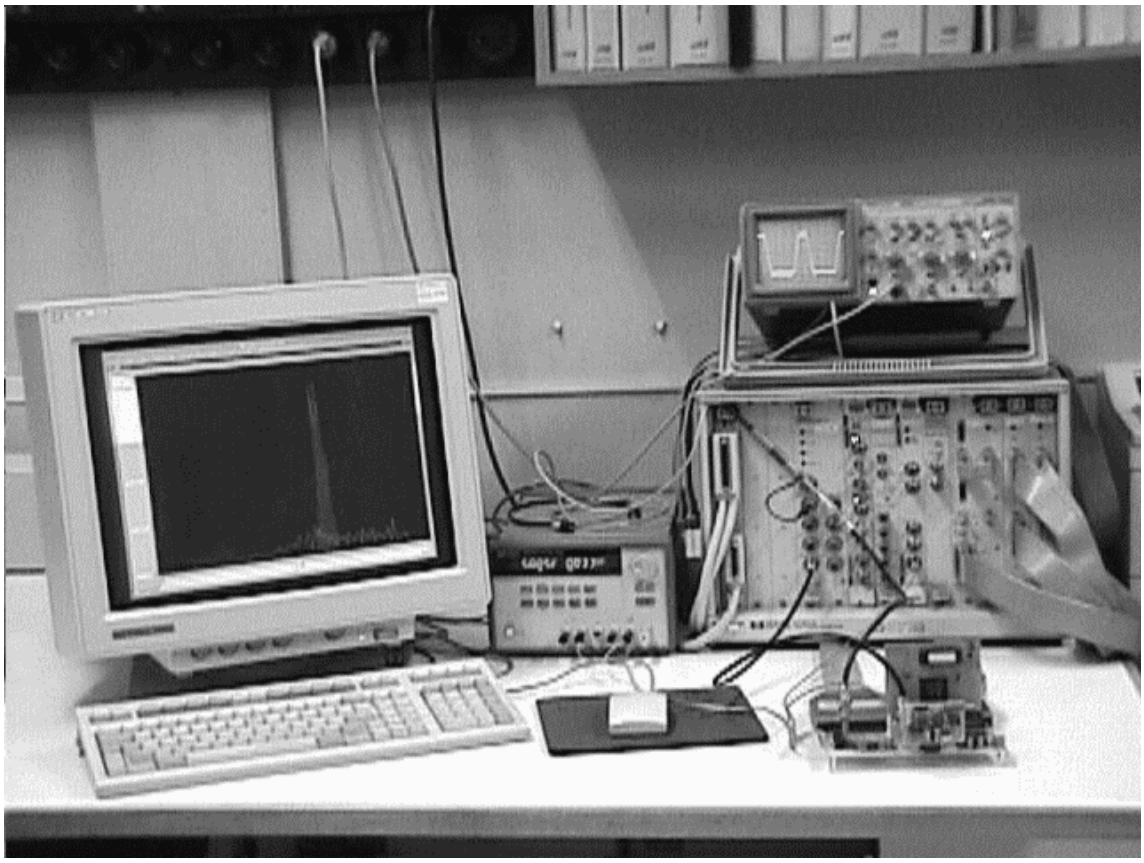

Figure 3. The view of the setup applied for efr measurement.

## 5. RESULTS OBTAINED

The Fig.4 and Fig.5 show the selected results that have been obtained for the flash ADC (TDA8703: 8bit/40MHz) and the pipelined ADC (TLC876C: 10bit/20MHz) respectively. All the three methods (traditional *IEEE*, heuristic *two-point*, and analytic *new*) have been applied in our investigation.

For a given ADC, the results of the efr measurement would ideally be the same, regardless of the particular DC offset $C$ and amplitude $V$ of the test signal (2) used in experiments. However all the three methods are not perfect and the variations in $C$ and $V$ cause variations in the efr measurements. A good measure of these variations is a histogram as, in the ideal case, it should be of a "delta" type at or very close to the nominal resolution. This technique is correct for the *new* method, Fig.4a and Fig.5a, when only the four most significant bits of the captured records are analyzed. In this case the maximum differential nonlinearity DNL is very small and both tested ADCs can be treated as perfect ones. The histogram obtained with the *IEEE* method shows that the measurement results are highly non-repeatable, and many of them are worthless, as often the efr $> 16$. The *two-point* method exhibits medium quality.

When we analyze the six most significant bits of the captured record the maximum differential nonlinearity is approximately four times higher than in the previous case, Fig.4b and Fig.5b. Hence the efr is evidently smaller than the nominal resolution of $R = 64$. It is true for the *new* and *two-point* methods, yet their distributions is spread over a small interval. This is caused mainly by the influence of a higher differential nonlinearity. Note that the results obtained by the *IEEE* method are again unusable and hardly repeatable, as sometimes efr $> 64$.

If the differential nonlinearity is of the order 0.5 LSB (that is 50%) all the three methods produce comparable (but not very good) results, Fig.4c and Fig.5c. The differential nonlinearity dominates the effect of better estimates and masks the effects created by the quantization error bias. The 8 bit converter ($195 <$ efr $< 205$) does not look much worse than the 10 bit converter ($200 <$ efr $< 215$). It means that the specification of the latter is rather optimistic.

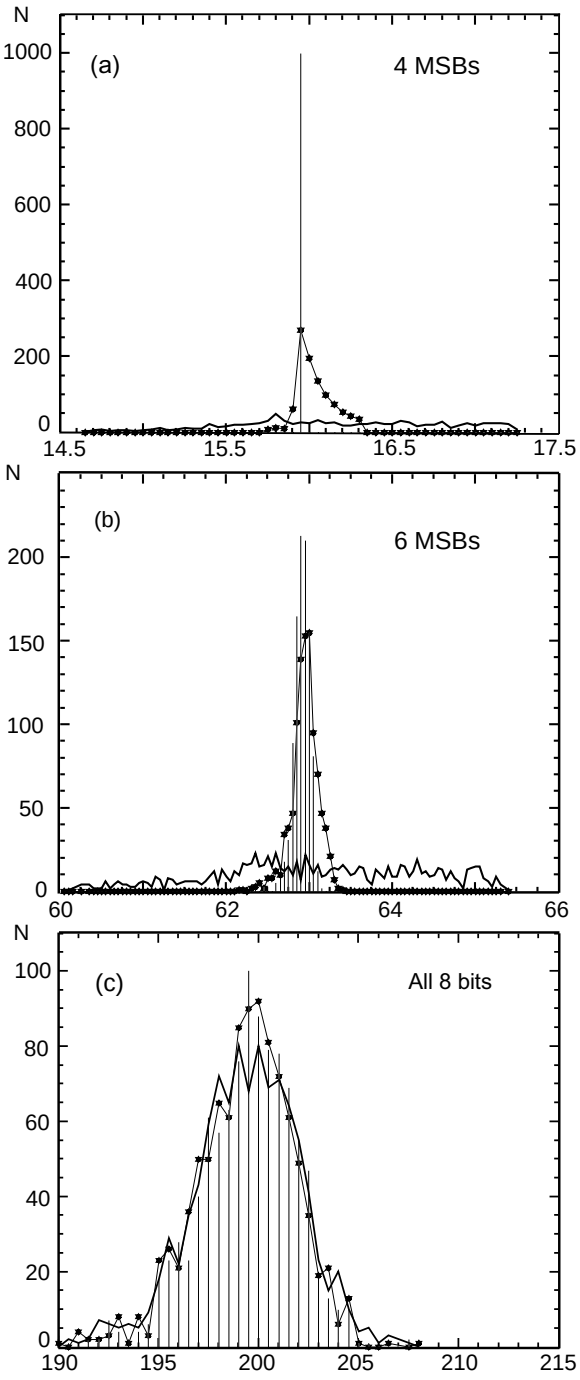


Figure 4. Effective resolution verification of the flash ADC (TDA8703 8bit/40MHz): $*$ – two-point method, thin lines – analytic method, thick line – IEEE method.

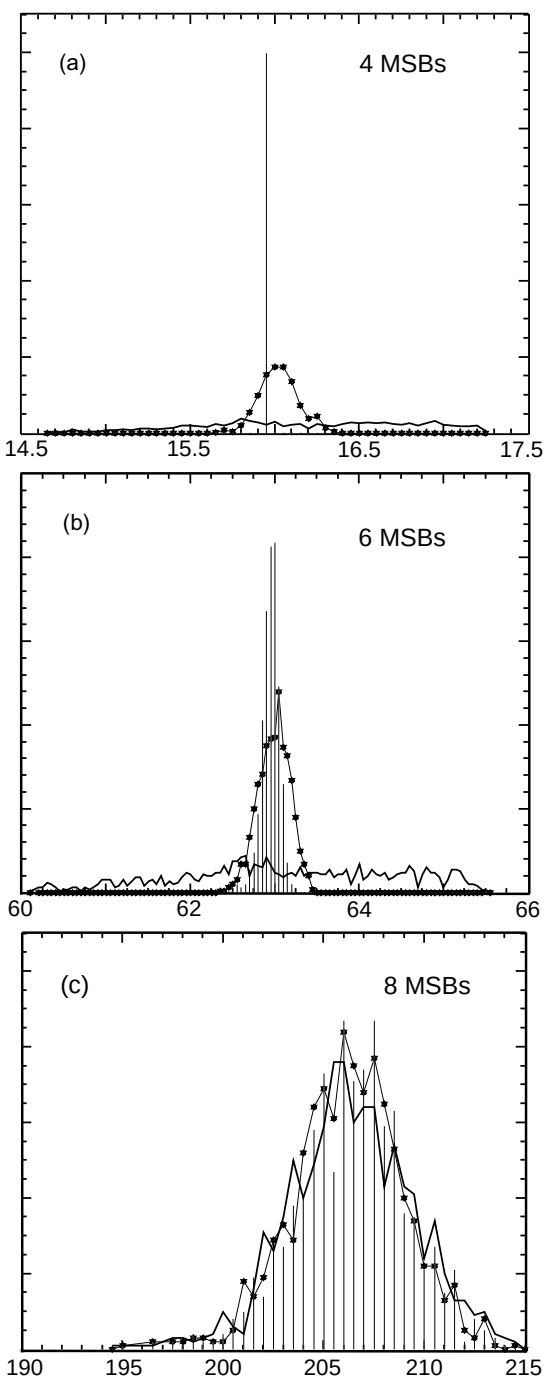


Figure 5. Effective resolution verification of the pipelined ADC (TLC876C 10bit/20MHz): $*$ – two-point method, thin lines – analytic method, thick line – IEEE method.

## 6. CONCLUSIONS

The equations (4) and (5) had not been developed at the beginning of the research described in this paper. At that time we used the heuristic *two-point* method [7] and applied the estimates (12) and (13). The measurement results agreed well with earlier simulations, but their repeatability for *accurate* ADCs were not satisfactory. It therefore appeared that further theoretical investigation was necessary [12]. The investigation resulted in the development of a fully analytic method for computing DC offset $C$ and amplitude $V$ estimates of a sinusoidal stimulus.

The quality of the *new* efr estimates have been comparatively verified with the hitherto existing *IEEE* definition by means of *hundreds of thousands* experiments. The *new*, proposed here, definition (9)

produces smaller bias and smaller variance of the efr measurements. Hence one can select the best ADC by the help of number comparison (that is by an *objective* manner). Moreover the *new* definition reminds in agreement with the theory of the perfect ADC, that is with very small differential nonlinearity.

The *new* method's efficiency comes from the exact estimate of the input test signal (2). This leads to *repeatable* results that are independent on measurement conditions (including the DC offset $C$ and amplitude $V$ temperature drift). Hence the *new* analytic method could be included into the text of the current norm [3] as well as into the text of the norm [4] presently under development.

The *new* method relies (between others) on solving the system of two non-linear equations (4, 5) for given $\overline{y}$ and $\overline{y^2}$. Both $\overline{y}$ and $\overline{y^2}$ are continuous functions of the DC offset $C$ and amplitude $V$ but their partial derivatives are discontinuous [5]. This fact usually forces a complicated iterative process but it is not necessary in this particular case. The well known initial conditions (10) and (11) lie close to the solution. So the functions (4) and (5) can be tabulated first and then analyzed for solution.

The problem of using other than sinusoidal stimuli, eg several sine waves (most promising results), white noise, triangle signal, etc is still an open question.

In summary, we would like once again to state clearly, that the conducted empirical research was preceded with many years of theoretical investigations and simulations. The research mentioned significantly simplifies all experiments that have been necessary for the verification of the *new* method proposed and gives yet better measuring results than the previous *two-point* method [7]. The global parameter of efr is useful for an ADC with a maximum differential nonlinearity up to 10%. If the nonlinearity reaches 50% or more the efr should be treated as a statistical concept and should be specified by its distribution.

The results of the presented investigations are addressed primarily to the members of the TC10 and EUPAS committee, and also to designers and users of computer-aided electronic systems.

# References

[1] B. Widrow, "Statistical analysis of amplitude-quantized sampled data system," *Trans. AIEE, Pt. II, Application and Industry*, vol. 79, Jan. 1961, pp. 555–569.

[2] K. Hejn and A. Pacut, "Generalized model of the quantization error — a unified approach," *IEEE Trans. Instr. Measurement*, vol. IM-45, Feb. 1996, pp. 41–44.

[3] "IEEE Std 1057, Standard for Digitizing Waveform Recorders," June 14 1994.

[4] "IEEE Std 1241, Standard for Terminology and Test Methods for Analog-to-Digital Converters," May 12 1997. Draft version.

[5] K. Hejn and A. Pacut, "Improved definition of adc effective resolution," 2000. Submitted to Elsevier.

[6] K. Hejn and A. Pacut, "Error correction in effective resolution measurement," in *IEE Conf. Publication on "Advanced A/D and D/A Conversion Techniques and their Applications", No.466*, (Glasgow, UK), University of Strathclyde, 27–28 July 1999, pp. 70–73.

[7] K. Hejn, A. Pacut, and L. Kramarski, "The effective resolution measurements in scope of sine-fit test," *IEEE Trans. Instr. Measurement*, vol. IM-47, Feb. 1998, pp. 45–50.

[8] Hewlett Packard, *HP 1489 MXIbus Controller Interface for HP 9000 Series 700 Workstations*, 1994. Installation Guide and Overview.

[9] K. Hejn, J. Jędrachowicz, A. Leśniewski, A. Pacut, and S. Sobczak, "Effective resolution measurement of mixed-signal circuits in the environment of MXI interface and C-SCPI precompiler." Project report KBN 8 T10C 025 14, 2000. In Polish.

[10] Hewlett Packard, *HP Compiled SCPI for HP-UX. User's Guide*, 1994.

[11] SCPI Consortium, *Standard Commands for Programmable Instruments (SCPI)*, 1994.

[12] K. Hejn, *Selected issues in the metrology of contemporary analog-to-digital converters.* Prace Naukowe, Elektronika z. 121, Warszawa: Oficyna Wydawnicza Politechniki Warszawskiej, 1999. In Polish.