XVI IMEKO World Congress
Measurement - Supports Science - Improves Technology - Protects Environment ... and Provides Employment - Now and in the Future
Vienna, AUSTRIA, 2000, September 25-28

THE PERFORMANCE TEST OF THE AD CONVERTERS EMBEDDED ON SOME MICROCONTROLLERS

R. Holcer
Department of Electronics and Telecommunications,
Technical University of Košice,
Park Komenského 13, SK-04120 Košice, Slovakia

Abstract: The paper deals with some metrological parameters of the ADC implemented on AT90S8535 and ADuC812 microcontroller chips. As a criterion of ADC precision, which allows to determine the operational condition limits, the number of effective bits has been chosen. More over, the DNL and INL measured characteristics are presented. The results are compared to some of the data brought out in vendors' data sheets.

Keywords: ADC performance testing, ADC errors and precision, microcontrollers,.

1 INTRODUCTION

Presently, the microcontrollers with analogue to digital converters (ADC) implemented on single chips and necessary analogue signal conditioning pre-processing blocks are very useful tools to design intelligent sensors. The aim of such structures is to recover the sensor's output signal as close as possible to the acquisition point in order to reduce the parasitic quantity impact. Acquired data are digitised, linearised, encoded and in the suitable format transmitted to the supervising computers which control the measuring process. Some of such microcontrollers possess general purpose voltage inputs. These inputs are sophisticated for the applications, where an additional analogue pre-processing circuit converts any output value from sensor into the ADC convenient voltage range.

2 ADC TESTING METHODS

The ADC implemented in tested microcontrollers contains a sample and hold circuit and these make possible to use dynamic testing methods in accordance with the IEEE Std. 1057 [1]. The dynamic testing methods have been chosen for testing number of effective bits (ENOB) as well as for testing differential and integral non-linearity (DNL, INL). All methods enable to utilise the harmonic generator with low harmonic distortion and medium frequency stability. The total harmonic distortion (THD) of test signal can be improved by a low pass or band pass filter. For testing the ENOB the sine wave fitting test method has been chosen for various input frequencies. The medium time frequency stability of the test generator enables to approximate parameters of the harmonic signal from acquired sample data by the four parameter method [1, 8]. Finally, the ENOB can be calculated from acquired and processed data. The histogram method with a sine wave input signal was used for measuring the DNL and INL. The obtained histogram was linearised by comparing to the ideal sine wave histogram and then the DNL and INL was calculated [1, 7]. The Pentium based PC with National Instrument card Lab-PC-1200 was applied to control the test process. The process of repeated continual AD conversions was started and stopped through this card. The results of AD conversions were moved to the PC across its strobed input data bus. A function/arbitrary waveform generator HP33120A (Hewlett Packard) was used for generating of harmonic input signals. Moreover, a simple optional RC low pass filter was applied to improve THD at the ADC input. The filter cut-off frequency was chosen and changed in relation to the harmonic test signal frequency. Sampling frequency was given by the microcontroller program and derived from the microcontroller crystal oscillator by an internal timer, if it was needed. A microcontroller software was written, debugged and compiled in the supervising PC by the developing software tools and then the microcontroller was programmed. The test controlling, data processing and presentation software for PC was fully developed in LabWindows/CVI programming environment (National Instruments).

3 ADuC812 MICROCONVERTER

The ADuC812 by Analog Devices [3] is a fully integrated 12-bit data acquisition system incorporating a high performance self-calibrating 8-channel ADC, dual 12-bit DACs and programmable 8-bit MCU (8052 instruction set compatible) on a single chip. It also provides following features:

8K bytes FLASH/EE program memory, 640 bytes FLASH user memory, 256 bytes data SRAM, 32 I/O lines, three timer/counters, internal and external interrupts, I^2C, SPI and Standard UART serial ports, Watchdog Timer, Power Supply Monitor, ADC DMA functions, On-Chip Temperature Sensor, three operating modes (Normal, Idle, Power-down) for the MCU core and ADC. The on-chip oscillator is driven by connecting an external crystal (max. 16M Hz). The part is specified for 3 V and 5 V operation.

3.1 ADC circuit information

The ADC conversion block provides the 8-channel mux, track/hold, on-chip reference, calibration features and A/D converter. The A/D converter consists of a conventional successive-approximation converter based on a switched capacitor DAC. The converter accepts an analogue input range of 0 to $+V_{REF}$. A high precision, low drift and factory calibrated 2.5 V reference is given on-chip. The internal reference may be overdriven via the external V_{REF} pin. The ADC has been designed to run at a maximum speed of 1 sample every 5 μs. (i.e. 200 kHz sampling rate). Total conversion time is calculated by following formula:

TCT = acq. time + conv. time ,

where acq. time = [1, 2, 3, 4] / ADC_{CLK} , conv. time = 16 / ADC_{CLK} , $ADC_{CLK} = M_{CLK}$ / [1, 2, 4, 8] ,

where (M_{CLK} = XTAL).

Single step or continuous conversion modes can be initiated in software or alternatively by applying a convert signal to the external pin. Timer 2 can also be configured to generate a repetitive trigger for ADC conversions. The ADC may be configured to operate in a DMA Mode whereby the ADC block continuously converts and captures samples to an external RAM space without any interaction from the MCU core. The ADuC812 is shipped with factory programmed calibration coefficients which are automatically downloaded to the ADC on power-up ensuring optimum ADC performance. The ADC core contains automatic end point self-calibration and system calibration options that will allow the user overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used. The basic specifications of ADC are referred in tab. 5.

3.2 Testing process and experimental results

The test was executed on the microcontroller implemented on the evaluation board EVAL-ADuC812QS by Analog Devices [4] with crystal frequency equal to 11.0592 MHz. Input operate amplifier was disconnected and the testing signal from waveform generator was connected directly to ADC input pin of microcontroller via RC filter. The original power supply source (the board accessory) was utilized for measuring and the internal reference V_{REF}=2.5 V was used as the ADC voltage reference. The ADC was tested in all conversion modes but this paper presents only the mode with the best results - continuos DMA conversion mode by using data memory on board and MCU core in IDLE operating mode. The tab. 1 and the fig. 3 showed the best measured results from all setting of the acquisition time for all possible setting ADC_{CLK}. The tab. 2 showed the dependent ENOB on acquisition time for one ADC_{CLK}. The fig. 1 and the fig. 2 showed result of DNL and INL testing, where f_{IN}=3.3 Hz, $ADC_{CLK}=M_{CLK}/8$ and ADC used timer 2 for repetitive trigger, then f_{SAMP}=27,1 kHz.

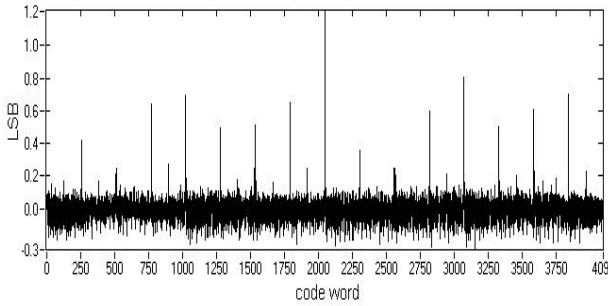

Figure 1. Differential non-linearity of ADuC812.

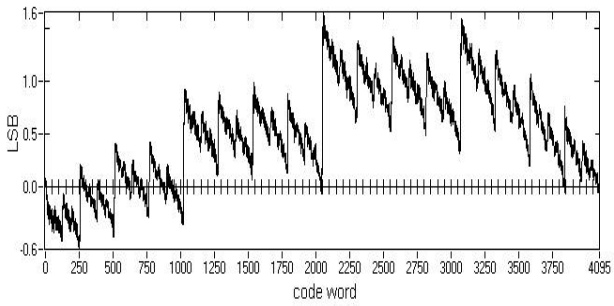

Figure 2. Integral non-linearity of ADuC812.

Table 1. Results of ENOB test of AduC812 for various ADC_{CLK}.

ADC_{CLK}	M_{CLK} / 8	M_{CLK} / 4	M_{CLK} / 2	M_{CLK} / 1
acq. time	2/ADC_{CLK}		4/ADC_{CLK}	
f_{SAMP} [Hz]	76800	153600	276481	526631
f_{IN}[Hz]	ENOB [bit]			
11	11.24			
33	11.27	11.25		
110	11.25	11.29	8.11	
330	11.28	11.29	8.10	5.35
1100	11.24	11.29	8.09	5.33
3300	11.22	11.27	8.10	5.35
11000	10.81	10.86	8.08	5.32
33000	9.89	9.89	8.03	5.34
66000	9.39	9.37	7.95	5.32
75000		9.30	7.94	5.36
110000			7.91	5.31
135000			7.89	5.16
260000				5.31

The sampling frequencies in the last two columns are higher than specified maximal sampling frequency 200 kHz.

Table 2. Results of ENOB test of AduC812 for various acq. time and for one ADC_{CLK} =M_{CLK}/8.

acq. time	4/ADC_{CLK}	3/ADC_{CLK}	2/ADC_{CLK}	1/ADC_{CLK}
f_{SAMP} [Hz]	69120	72758	76800	81318
f_{IN}[Hz]	ENOB[bit]			
11	11,13	11,13	11,24	11,15
33	11,19	11,18	11,27	11,17
110	11,13	11,15	11,25	11,16
330	11,17	11,18	11,28	11,17
1100	11,15	11,15	11,24	11,17
3300	11,13	11,13	11,22	11,12
11000	10,78	10,80	10,81	10,75
15000	10,62	10,54	10,59	10,55
25000	10,16	10,10	10,12	10,10
33000	9,89	9,88	9,89	9,87

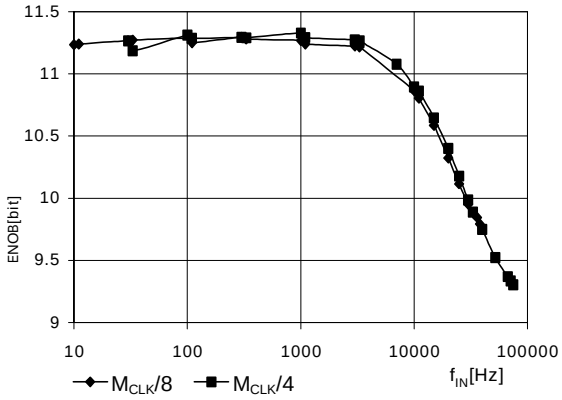

Figure 3. ENOB of ADuC812 for various ADC_{CLK}.

Without IDLE mode the ENOB is lower by about 0.3 LSB in the all conversion mode. Also an activity of internal timers causes decreasing of ENOB. For example, when the ADC was triggered by timer 2 (acq. time = 4/ADC_{CLK} , ADC_{CLK} = M_{CLK}/8 , without DMA, without IDLE) and timers 0, 1 were also active, maximal ENOB was 10.8 bits. The testing ADC with battery supply source had better results by about 0.2 bits. Shapes of measured characteristics are identical for all conversion modes, however the absolute values depend on the disturbing factors mentioned higher.

4 AT90S8535 MICROCONTROLLER

The AT90S8535 by ATMEL [2] is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. It provides the following features: 8K bytes Flash program memory, 512 bytes data EEPROM, 512 bytes data SRAM, 32 I/O lines, 32 working registers, three timer/counters, internal and external interrupts, SPI and standard UART serial ports, 8-channel, 10-bit ADC, 3 PWM Channels, On-Chip Analogue Comparator, Real Time Clock, Watchdog Timer, three power saving modes (Idle, Power down, Power save). Maximal frequency of crystal is 8 MHz. The operating voltage is from 4.0 V to 6.0 V.

4.1 ADC circuit information

The AT90S8535 features a 10-bit successive approximation ADC, 8-channel multiplexer and a Sample/Hold Amplifier. An external reference voltage must be applied to the A_{REF} pin. This voltage must be in the range AGND - AV_{CC} . The ADC can operate in single or free run conversion mode. In the first mode, each conversion will have to be initiated by the user. In second mode, the ADC is constantly sampling and updating the ADC data register. The ADC contains a prescaler, which divides the system clock to an acceptable ADC clock frequency:

ADC_{CLK} =M_{CLK} / [2, 4, 8, 16, 32,64,128]

The ADC accepts input clock frequencies in the range 50 - 200 kHz, then total conversion time is 65 – 260 µs. The sample/hold activity takes 1.5 ADC clock cycles after the start of the conversion. The one conversion is ready after 14 ADC clock cycles in single mode and 13 in free run mode. Using Free

Run Mode and an ADC clock frequency of 200 kHz gives the lowest conversion time, 65μs, equivalent to 15.4 kSps. To improve noise reduction, the vendor recommends the Sleep mode of the microcontroller, when the core activities are stopped during the AD conversion. The basic specifications of ADC are referred in tab.5.

4.2 Testing process and experimental results

The test was executed on microcontroller with crystal frequency equal to 8 MHz. The testing harmonic signal from waveform generator was connected directly to ADC input pin of microcontroller via RC filter. As the external voltage reference V_{REF}=2.5 V was used integrate circuit AD680 (Analog Devices). The ADC was tested in both conversion modes. The results of ENOB for ADC in single conversion mode triggered by timer 1 for all possible setting ADC_{CLK} are presented in the tab. 3 and the fig. 4. The tab. 4 and fig. 5 present results for same test but ADC is set in free run mode (without timer 2). The fig. 6 and the fig. 7 showed result of DNL and INL testing, where f_{IN}=3.3 Hz, $ADC_{CLK}=M_{CLK}/32$ and free run mode.

Table 3. Results of ENOB test of AT90S8535 in single conversion with timer 1 for various ADC_{CLK}.

ADC_{CLK}	$M_{CLK}/128$	$M_{CLK}/64$	$M_{CLK}/32$	$M_{CLK}/16$	$M_{CLK}/8$
f_{SAMP} [Hz]	3846	7693	15391	15391	15391
f_{IN}[Hz]	ENOB [bit]				
≤ 3,3	9,36	9,37	9,46	9,38	9,41
11	9,32	9,35	9,39	9,34	9,34
33	8,91	9,12	9,14	9,13	9,13
110	7,91	8,60	8,94	9,06	9,11
300	6,59	7,53	8,34	8,88	9,14
330		7,41	8,23	8,83	9,14
1000		5,87	6,85	7,89	9,13
1100			6,72	7,78	9,12
3000			5,30	6,44	9,11
30000					8,87
63000					8,33

The ADC_{CLK} in the last three columns are higher than specified maximal 200 kHz.

Table 4. Results of ENOB test of AT90S8535 in free run mode for various ADC_{CLK}.

ADC_{CLK}	$M_{CLK}/128$	$M_{CLK}/64$	$M_{CLK}/32$	$M_{CLK}/16$	$M_{CLK}/8$
f_{SAMP} [Hz]	4808	9616	19233	38337	76935
f_{IN}[Hz]	ENOB [bit]				
≤ 3.3	9,40	9,44	9,41	9,33	9,39
11	9,37	9,40	9,36	8,88	9,41
33	9,17	9,20	9,13	7,75	9,21
100	9,13	9,13	9,11	5,85	9,16
300	9,14	9,14	9,12		9,17
1000	9,04	9,09	9,08		9,15
3000	9,14	9,10	9,02		9,05
10000		9,06	8,98		9,13
30000		8,97	8,85		8,79
60000		8,38	8,39		8,30
90000		7,78	7,94		7,91
130000			7,47		7,41
250000					6,59

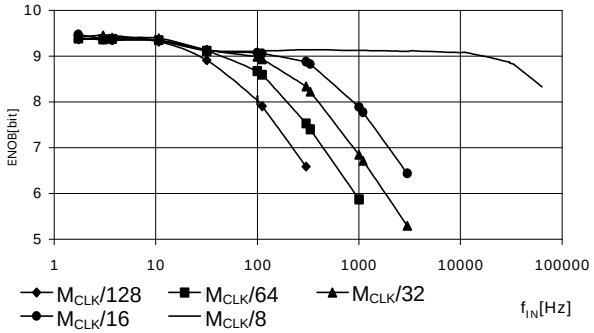

Figure 4. ENOB of AT90S8535 in single conversion with timer 1 for various ADC_{CLK}.

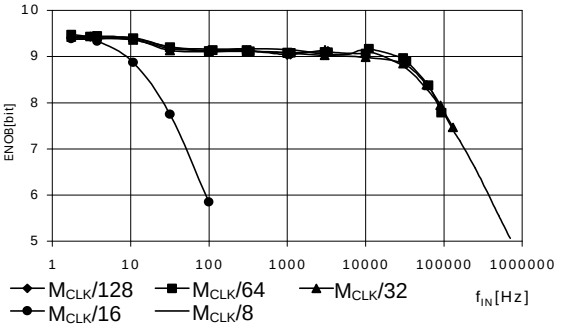

Figure 5. ENOB of AT90S8535 in free run mode for various ADC_{CLK}.

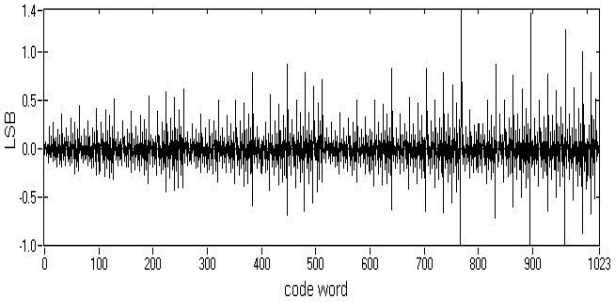

Figure 6. Differential non-linearity of AT90S8535.

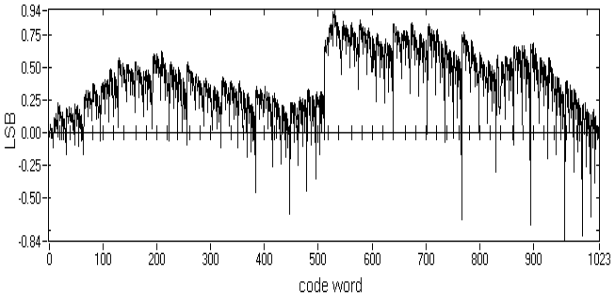

Figure 7. Integral non-linearity of AT90S8535.

The ADC conversion was not executed correctly when the ADC_{CLK} was equal $M_{CLK}/4$ or $M_{CLK}/2$ (ADC_{CLK} was too high). ADC testing with supply from various power sources (power range $AV_{CC}=V_{CC}$ from 2,8 V to 5,5 V) hasn't indicated any influence of power source on ENOB. Even an application of battery supply source hasn't brought any advance.

4 CONCLUSION

The mutual comparing of ADC parameters is very difficult, because the resolution of ADCs implemented on tested microcontrolers is different. Some of these parameters are presented in tab. 5. However these ADCs can be compared from other point of view. Experiments with microconverter ADuC812 confirmed high time punctuality of its triggering circuit. Also the microcontroller AT90S8535 has similar precise time triggering but only in free run mode. In repeated triggered single conversion mode controlled by any timer a triggering jitter was indicated. It depends on run-time optimisation of ADC start conversion subroutine. More over, the ADuC812 gives more ADC options than AT90S8535. The experimental results from testing ADC implemented on AduC812 are most coherent to the expected error model of SAR ADC described in [5], [6] than those from similar AD converter embedded on microcontroler AT90S8535.

Table 5. Comparison table of ADC specifications.
$AV_{DD}=DV_{DD}=AV_{CC}=V_{CC}$ =5 V, V_{REF}=2.5 V

		AduC812		AT90S8535	
		by vendor	Measured	by vendor	measured
Resolution		12 bits		10 bits	
ENOB			11.3 bits		9.45 bits
Integral non-linearity	(typical)	±0.5 LSB		±0.2 LSB	
	(maximal)	±1.5 LSB	1.6 LSB	±0.5 LSB	1.4 LSB
Differential non-linearity	(typical)	±1 LSB		±0.2 LSB	
	(maximal)		1.2 LSB	±0.5 LSB	0.95 LSB
Signal to Noise Ratio (SNR)		70 dB	69.7 dB		58.7 dB

REFERENCES

[1] IEEE Std. 1057 - 1994, "IEEE Standard for Digitizing Waveform Recorders", *Institute of Electrical Engineers*, Inc. New York, USA 1994
[2] Preliminary Datasheet of ATMEL 8 bit AVR microcontrollers AT90S4434/AT90LS4434/AT90S8535/ AT90LS8535, Rev. 1041E–04/99, Atmel Corporation 1999. (See also http://www.atmel.com)
[3] Preliminary Datasheet of Analog Devices MicroConverter ADuC812, REV. PrD Nov. /98, Analog Devices, Inc. 1998. (See also http://www.analog.com)
[4] ADuC812 52PQFP Applications board user guide, Version 3.00, 30. March 1999, Analog Devices, Inc. 1999. (See also http://www.analog.com)
[5] L, Michaeli, J. Šaliga, "An educational application of distributed measurement systems", *Radioengineering Vol.4.,No5,* April, 1999, p. 20-24, ISSN 1210-2512
[6] P. Arpaia, P. Daponte, L. Michaeli, "The influence of the architecture on ADC modelling", *IEEE Trans.on Instrumentation and Measurement, Vol 48., No.5.*, October, 1999, p. 956-967, ISSN 0018-9456
[7] J. Holub, J. Krecl, J. Vedral, "Full-test of performance of AD input in single-chip microcontrollers", *Proceedings of IMEKO ISDDMI'98 International Symposium* (Naples, 17-18.September 1998), Naples, Italy, 1998, p. 441-443.
[8] L, Michaeli, J. Saliga, V. Sedlak, "An approach to diagnostic of the AD converter embedded on ATMEL microcontrollers", *Proceeding of IMEKO IWADC'99, 4th International Workshop on ADC Modeling and Testing* (Bordeaux, 9-10. September 1999), Bordeaux, France, 1999, p. 247-252.

AUTHOR(S): Ing. Roland Holcer, Department of Electronics and Telecommunications, Technical University of Košice, Park Komenského 13, SK-04120 Košice, Slovakia, Phone (421) 95 6022853, Fax (421) 95 6323989, E-mail: holcer@tuke.sk