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LARGE SCALE ERROR REDUCTION IN DITHERED ADC

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Abstract: The combination of dithering and correcting table is the way of improvement not only of ADC resolution but also of linearity - effective number of bits. Dithering is used to reduce small-scale errors, such as quantization error, while correcting table reduces large-scale errors.

The contribution describes design and practical experience with ADC unit based on single-chip micro-controller 80C552 that uses above described correction procedure. Sub-quantum accuracy has been achieved.

Keywords: Analogue-to-Digital Converter, Dithering, Large Scale Errors

1 INTRODUCTION

Dithering, which means adding of a defined signal to the input, is a well-known method that can be used for reduction of small-scale errors (such as the quantizing one) of Analogue-to-Digital Converters [1]. Thus, resolution can be enhanced rather easily. Unfortunately, also the Large-Scale Error (LSE) distorts the output of the ADC. These errors can not be simply reduced by dithering and become a reason of impossibility of Effective Number of Bits ($ENOB$) enhancement above a certain level, which is usually not higher than 1 or 2 bits above the nominal number of bits of the used ADC [2].

To overcome these difficulties, it is necessary to introduce a LSE reducing algorithm. One suitable method is the look-up table that saves INL (Integral Non-linearity) values of the dithered ADC. The combination of dithering and look-up table has been proposed in 1998 [3].

2 THEORY OF DITHERING

The most efficient method of dithering is to add to the signal a series of N values that are distributed uniformly on the range (-q/2, q/2). It is easy to show that this method applied to a steady measurand and averaging *N* samples for each result gives the Effective Number of Bits (*ENOB*)

$$ENOB = n + \log_2 N \tag{1}$$

where n is the nominal number of bits of the used A/D converter [2]. When the dithering signal is distributed on a larger range (an exact multiple of LSB has to be covered to provide unbiased result), the enhancement of $ENOB$ is lower than (1) indicates, but the smoothness of the DNL (Differential Non-linearity) of the used A/D converter is better. There are several types of deterministic signal with uniformly distributed probability function, such as the periodic ramp or sawtooth signal. These are difficult to generate precisely (with high linearity and stability) at a reasonable cost. Thus, a different signal with similar distribution has been found for the application.

PWM (Pulse-Width Modulation) output of a microcontroller is available. It can provide a logic signal at CMOS level 0/5 V with variable frequency and duty factor. This signal with suitable frequency 1/(2T) and duty factor 0.5 (U_{max} = 5 V for a time interval T and then U_{min} = 0 V for the following time interval T) serves as the input signal for the passive RC low-pass with time constant $\tau = RC$. The range of the output exponential signal is <U_{mean} - U_m, U_{mean} + U_m> where

$$U_m = \frac{U_{max} - U_{min}}{2} \cdot \frac{1 - e^{-\frac{T}{t}}}{1 + e^{-\frac{T}{t}}} \tag{2}$$

and U_{mean} is the mean value of output signal,

$$U_{mean} = \frac{U_{max} + U_{min}}{2} \tag{3}$$

(in this case 2,5 V). The probability density function is

$$f(x)=\frac{t}{T}\cdot\frac{2}{U_{\max}-U_{\min}}\cdot\frac{1}{1-4\left(\dfrac{x-U_{\text{mean}}}{U_{\max}-U_{\min}}\right)^2} \qquad \text{for } \left|x-U_{\text{mean}}\right|\le U_{\text{m}}$$

$$\text{and } f(x)=0 \qquad \text{for } \left|x-U_{\text{mean}}\right|>U_{\text{m}} \tag{4}$$

The probability density function is for T << τ similar to the ideal uniform probability density function. The value of U_{m} is approximately

$$U_{\text{m}}=\frac{U_{\max}-U_{\min}}{2}\cdot\frac{1}{2a} \tag{5}$$

where $\alpha=\tau/T$. When considering the probability density function to be uniform, the maximal error appears at the marginal values (U_{mean} - U_{m}) and (U_{mean} + U_{m}), and its relative value is approximately

$$err(a)=\frac{1}{2a-1} \qquad (\cdot 100\%) \tag{6}$$

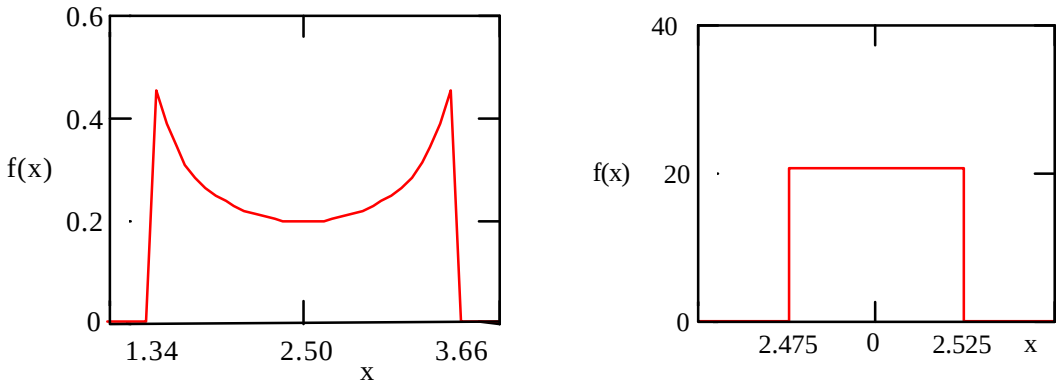

Fig.1 The probability density function of the signal (4) for t=T (left) and t=50T (right)

This means that the error is less than 1% for $\tau > 50T$, and the above described signal can be used for dithering instead of the ramp or sawtooth signal, which would require a more complicated generation using an active integrator or a D/A converter.

3 DESCRIPTION OF ADC UNIT FUNCTION

A block diagram of dithered measuring system, based on 80552, is depicted on Fig. 2. During one measuring cycle *m* periods (*m* must be an integer) of the logic signal are generated and *n* time-equidistant samples are acquired by the internal ADC. When *m* and *n* are relative prime, the situation corresponds to *n* time-equidistant samples within one period of dithering signal that are acquired *1/m*-times faster [1]. The other condition for design of parameters of the dithering signal is the maximal slew rate of the combined input signal that is 10 V/ms [4]. An average value of *n* samples is calculated.

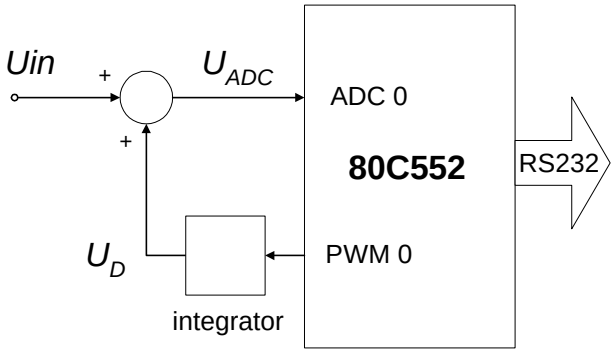

Fig.2 Schematic diagram of dithering application for 80552

The LSE reducing mechanism is explained in Fig.3. There is a table of recalculated INL values (c_i) saved in the controller memory. Table values are obtained during calibration phase using a standard histogram test [5]. Approximately 1000 samples are acquired per each code word during calibration using a sawtooth input signal, and values of INL (Integral Non-linearity) are calculated from DNL (Differencial Non-linearity). Then, the INL values are recalculated according to the *TEM* - Theorem of Equivalent Non-linearity. *TEM*, derived e.g. in [6], says: "For the purpose of calculation of conditional expectation any non-linearity *y(x)* with an input signal *s+n* is equivalent to another non-linearity *Y(x)* with *s* as its only input. Equivalent non-linearity *Y(x)* is determined by convolution of original transfer function *y(x)* with *PDF* (probability density function) of added component *n*".

In our case, the fact that error of resulting characteristics Y(x) is determined by convolution of error of original transfer function and *PDF* of added component *n* is used (this simple conclusion that can be easily derived from *TEM* is valid only for symmetrical *PDF*s with zero mean):

$$c_i = \sum_{j=-\infty}^{\infty} INL_j \cdot f(j-i) = \frac{1}{7} \sum_{j=i-3}^{i+3} INL_j \tag{7}$$

where *f*() is the discrete probability density function of the dithering signal (that is uniformly distributed in the area of 6 LSB with zero mean: *f* (-3) = *f* (-2) =…= *f* (3) = 1/7, otherwise 0).

The averaged output code word with extended length by dithering that corresponds to input voltage U_{in} is Q_d (see Fig.3). Let it be located between the original code words Q_i and Q_{i+1} with corresponding correction values c_i and c_{i+1}. The final output value Q_o is calculated using linear interpolation:

$$Q_o = Q_d + c_i + (c_{i+1} - c_i)(Q_d - Q_i) \tag{8}$$

Then, offset and gain errors are compensated using standard algorithms. Necessary correcting parameters are obtained during the initial calibration by measurement of the steady-state input calibration voltage and a zero input voltage.

4 ACHIEVED RESULTS

Two examples of achieved results are depicted in Fig.4 and Fig. 5, and listed in Tab.1. and Tab.2. Please note that the width of ideal code bin width of the original ADC is approximately 5 mV. Because INL values goes up to 6mV, the maximum conversion error of ADC without dithering and LSE reduction exceeds 8 mV.

Tab.1 The comparison between original and enhanced parameters (12b-res.) of ADC (on chip 80C552)

	ORIGINAL ADC	DITHERED ADC	DITHERED ADC WITH *LSE* REDUCTION
Input Full Scale [V]	5	4.98	5
(Effective) Sampling Rate [Sa/s]	12000	83	83
Output code length [bit]	10	12	12
Effective Resolution [bit]	9.8	11.8	11.8
ENOB [bit]	9.20	10.41	11.62

Tab.2 The comparison between original and enhanced parameters (16b-res.) of ADC (on chip 80C552)

	ORIGINAL ADC	DITHERED ADC	DITHERED ADC WITH *LSE* REDUCTION
Input Full Scale [V]	5	4.98	5
(Effective) Sampling Rate [Sa/s]	12000	8	8
Output code length [bit]	10	16	16
Effective Resolution [bit]	9.8	15.4	15.4
ENOB [bit]	9.20	11.52	13.97

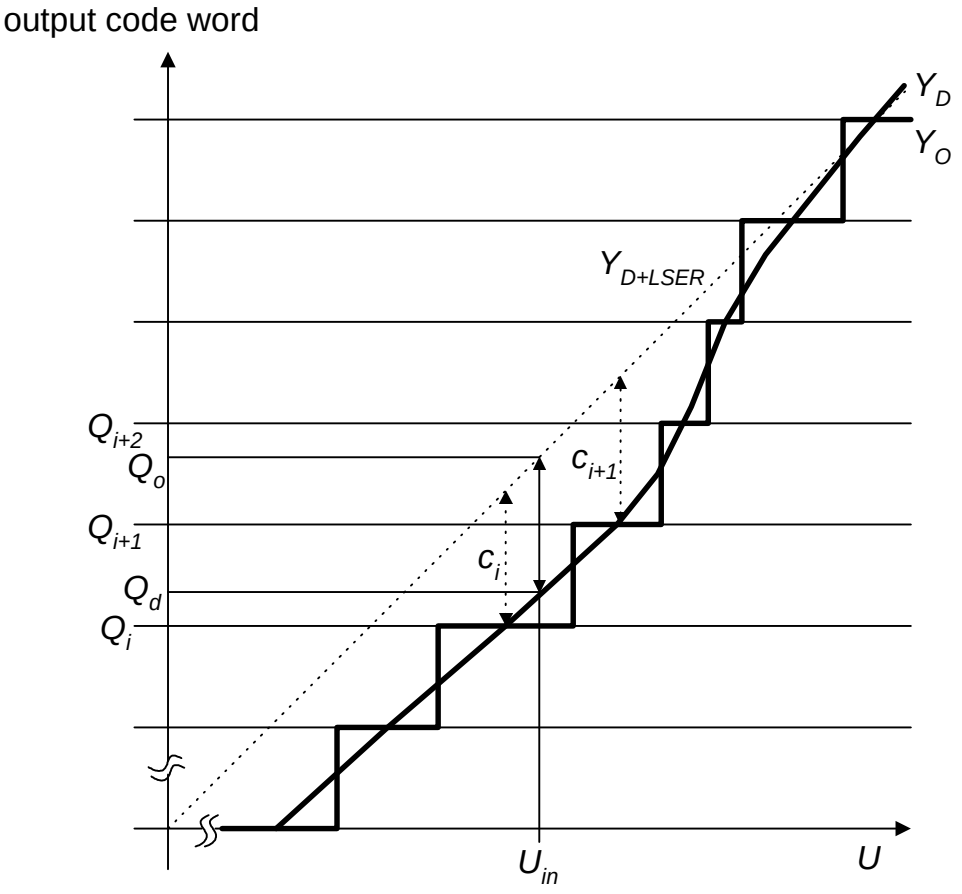

Fig. 3 Large Scale Error reduction

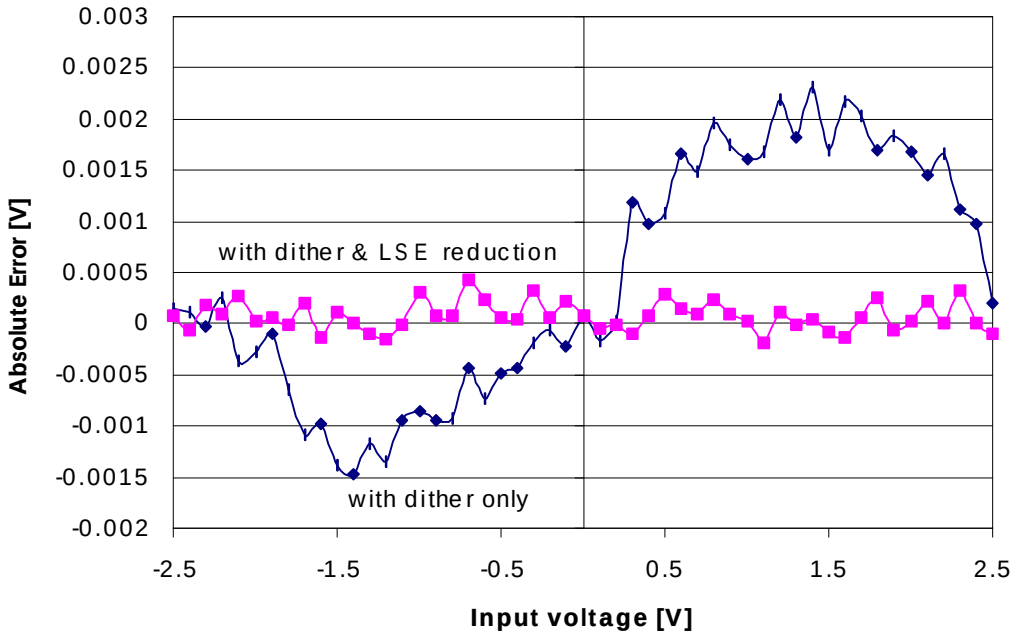

Fig. 4 Absolute error of conversion of dithered ADC with and without LSE reduction (12b resolution)

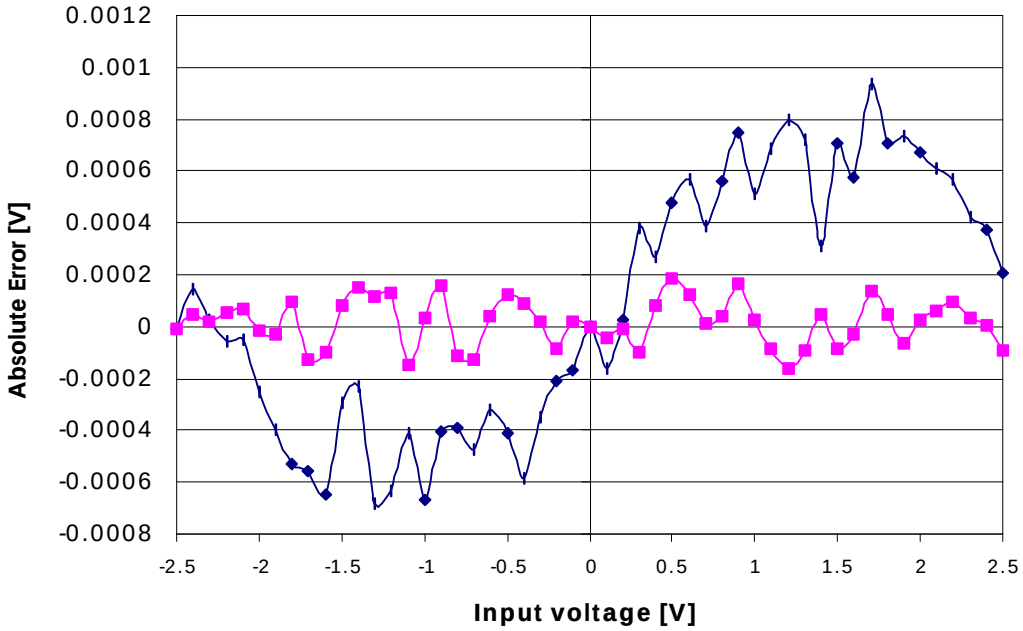

Fig.5 Absolute error of conversion of dithered ADC with and without LSE reduction (16b resolution)

The above listed parameters have been achieved by averaging of 64 (for 12bit-resolution) respectively 1024 (for 16bit-resolution) output code words, using triangular dithering signal covering 6 LSB and LSE-reducing correcting table containing 1023 values of recalculated INL. For the used type of ADC (successively approximating ADC on the 80C552 chip), given parameters are valid at least one

week after calibration process that takes approximately 20 minutes (histogram test and offset and gain calibration).

Note that the $ENOB$ has been calculated using the standard definition [5]

$$ENOB = \log_2 \frac{FS}{s\sqrt{12}} \tag{9}$$

where FS is the input full scale range and σ is the rms error of AD conversion. This rms error should be calculated using the set of input/output values that covers the whole characteristics of the AD converter using as many points as possible (10 per LSB or more). Such a requirement cannot be easily fulfilled, especially for high-resolution, low-speed ADCs. In our case, 50 randomly distributed values of input voltage have been measured (see Fig.4 and Fig.5). These values have covered the input range of ADC approximately uniformly.

5 CONCLUSION

The combination of dithering and static correction table can significantly enhance the linearity of ADC. Of course, the effective sampling rate is reduced. In our case, the linearity of 14 bits ($ENOB$) has been achieved using a nominally 10-bit ADC on the chip of a microcontroller 80C552. For comparison, dithering only (without correcting table) enables to achieve rarely better linearity than 2 bits above the nominal number of bits of used ADC. Usage of correcting table only (without dithering) can not bring a higher $ENOB$ than the nominal number of bits at all.

REFERENCES

[1] O. Aumala, J., Holub: Dithering Design for Measurement of Slowly Varying Signals. *Measurement*. **23**, No. 4, 1998, pp. 271-276

[2] J. Holub, J. Vedral: Dithered Quantizer of ADC Plug-In Card: Theoretical Model and Practical Testing. *Proc. XIV IMEKO World Congress: New Measurements - Challenges and Visions*. Vol. IVB. Helsinki: Finnish Society of Automation, 1997, pp. 287-290

[3] J. Holub, R. Smid: Visualisation and Reduction of Various Scale Errors in Dithered Quantizers, *Proc. ISDDMI 98 10th International Symposium on DEVELOPMENT IN DIGITAL MEASURING INSTRUMENTATION*. Naples: Faculty of Engineering, 1998, pp. 377-380

[4] J. Holub: A Novel Low-cost Dithering Application for ADC in Single-chip Microcontroller, *Proc. Internet Virtual Workshop Dithering in Measurement: Theory and Applications*, http://measure.feld.cvut.cz/dithering98, 1998, pp. 29-33

[5] IEEE-STD 1241 draft

[6] S. Dado: Dithering – a Special Case of Non-linearity Correction, *Proc. Internet Virtual Workshop Dithering in Measurement: Theory and Applications*, http://measure.feld.cvut.cz/dithering98, 1998, pp. 6-10

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