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SELF-SUBTRACTIVE DITHERING IN HIGH-RESOLUTION SIGMA-DELTA A/D CONVERTERS

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Abstract: An essential disadvantage of application of the oversapling sigma-delta A/D converters in high-resolution DC measuring systems are local peaks of quantization errors observed for some specific input signal values. The best method of elimination of those peaks is application of additional, deterministic, digitally generated dithering signal to the converter input. When averaging period of the converter digital output filter is a exact multiple of the period of the dither signal, this topology is intrinsically subtractive and elimination of DC residue is achieved without the need of additional digital subtraction. Experimental results of commercially available, nominally 24-bit sigma-delta converter with added simple self-subtractive circuit proved, that full elimination of the most significant peaks of errors was obtained. Increase of effective resolution of this converter (ENOB) was from 1,5 to 4 bits.

Keywords: Sigma-delta A/D converter, Oversampling, Dithering

1 INTRODUCTION

Local peaks of quantization errors, observed for same specific input signal values in all oversampling A/D converters, are connected with appearance of the specific sequences of output signals, called correlation codes. Those peaks considerably lowers effective resolution of the converters for particular values of DC input signals. In measurement systems, self-calibration procedures for removing offset and gain errors associated with input conditioner and A/D converter are usually executed at two external standard values on each instrument ranges (Fig. 1). On all DC measurement ranges, one standard value required for calibration is usually zero, and second is near full scale of the instrument [1]. Unfortunately, the most important zones of reduced accuracy are observed near zero (Fig. 2) and near full scale values of input signals. Therefore mentioned zones of reduced accuracy of oversampling converters in significant degree influences effectiveness of automatic calibration procedures and overall accuracy of the whole measurement system.

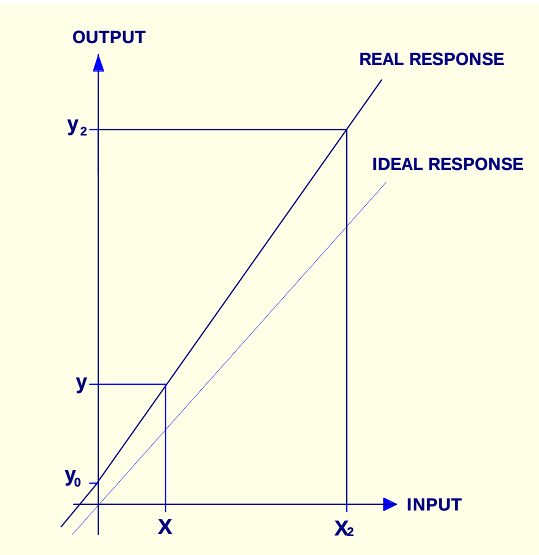

Fig.1. Transfer response of the converter
(x and x_2 - calibration values)

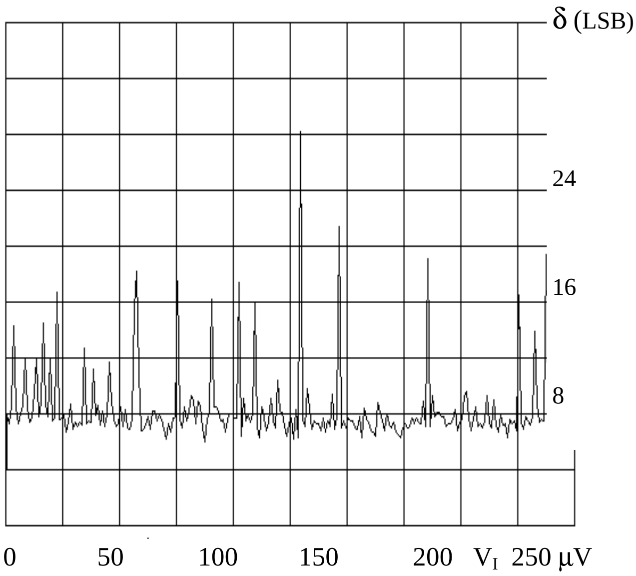

Fig.2. Conversion errors (effective values)
of nominally 24 bit sigma-delta converter
for low values of DC input without dither

The best method of reduction of this undesirable peaks of errors caused by correlation codes is application of the additional dithering signal to sigma-delta converter input. There are two known main methods of realization of the dithering in A/D oversampling converters [2...6]:

1. Non-subtractive dithering (Fig. 3a), usually realized by a stochastic dither signal with unknown instant values and properly shaped frequency spectrum, connected to input of the sigma-delta modulator;
2. Subtractive dithering (Fig. 3b), realized by means of the auxiliary digital to analog converter, controlled by the random, or pseudo-random number generator. Instant values of the dither signal are added to the input and their digital representations may be digitally subtracted from the output codes of the converter.

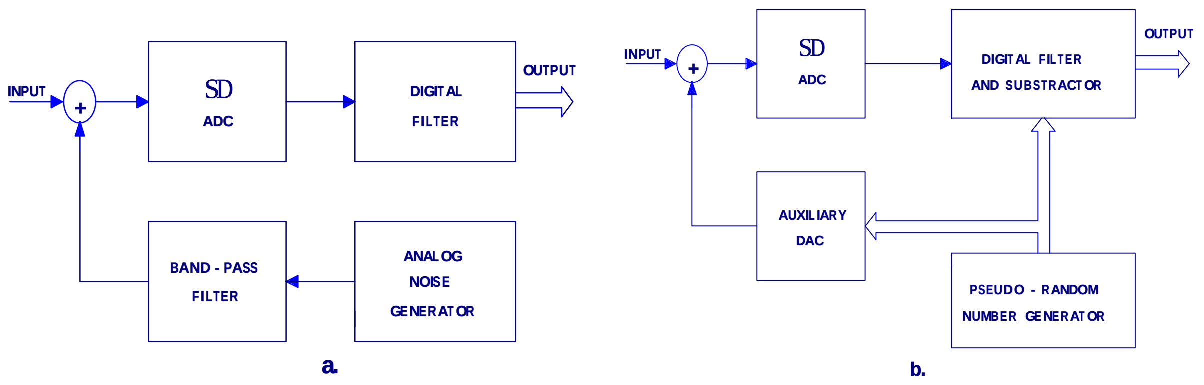

Fig. 3. Sigma-delta A/D converter with non-subtractive (a) and subtractive (b) dithering

In the non-subtractive dithering, average DC value of the dither signal, counted for averaging period of the output digital filter should be as small as possible. Remainders are directly added to the conversion output, causing instability and additional, random errors. The analogue filter, connected between dither signal generator and sigma-delta modulator input, should therefore effectively reject low frequency components of the generated signal. For sigma-delta application, the dither signal spectrum should be included between the transmission band of the output digital filter and sampling frequency of the converter modulator. For generation of noise dither signal, CMOS amplifier, connected to band-gap reference voltage source and additional analogue active filter for shaping signal frequency spectrum may be utilized [7]. It has been established, that for proper results amplitude of dithering signal should be low; and a signal of RMS value corresponding to 10 LSD (least significant digits) of a converter input turns out to be the best for reduction of the worst peak of conversion errors, observed for low input signal values.

2 SELF-SUBTRACTIVE DITHERING

Stochastic, non-subtractive dithering causes reduction of the worst peak of conversion errors, observed for particular input values, but for other input signals effective resolution of dithered converter may be even slight worse that without dither [7]. The subtractive dithering should be less sensitive for dither signal amplitude, but its realization with commercially available sigma-delta A/D converters and digital processors is not so simple. For that reason, in the experimental instrument, utilization of non-subtractive dithering with deterministic, pseudo-random, digitally generated signal was investigated. It was shown by Petri [4], that when averaging period of the digital output converter filter is a exact multiple of the period of the dither signal, this topology is intrinsically subtractive and dither subtraction of the average value of dither signal is achieved without the need of realization of digital subtraction of the instant values.

In experimental digital voltmeter with high-resolution oversampling A/D converter, build in Industrial Institute of Electronics, pseudo-random dither signal was generated by the additional 8-bit digital to analog converter driven by deterministic, periodic signals, which instant amplitudes were written in EPROM memory. In our circuit (Fig. 4) both periods (averaging period in the output filter and period of the dither signal generated by auxiliary digital to analog converter) are determined by the same clock generator CLK, which (with properly chosen values of counters capacity N and M) assure that output filter averaging period is exact integer of period of the signal generated by auxiliary D/A converter. The null remainder of dither signal in output filter averaging period is therefore assured.

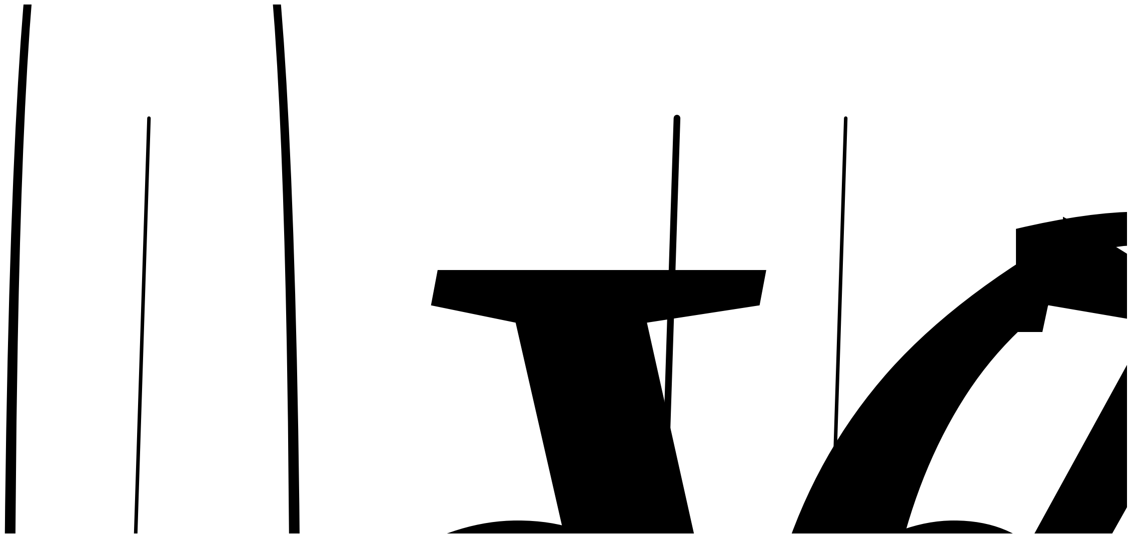

Fig. 4. Realization of the sigma-delta A/D converter with self-subtractive, deterministic dithering

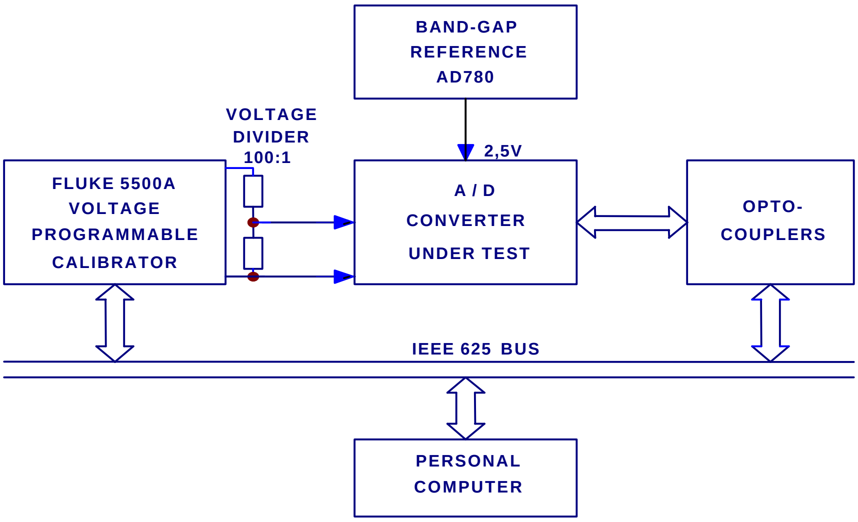

Fig. 5. Test circuit for testing dithered sigma-delta converters

3 EXPERIMENTAL RESULTS

For comparison of efficiency of various dithering methods, special test circuits with precision programmable voltage source, was build (Fig. 5). Input voltage of the tested converter was changed in very low, 100 nV steps. For each input value, digital results of several (from 100 to 1000) conversions was stored, and their mean value v_0 and standard deviation δ were calculated. In experimental system with self-subtractive dithering from fig. 4 commercially available, nominally 24 bit sigma-delta converter and simple 8 bit CMOS digital to analog converter were used. Instant values of dither signal was writhed in 256 X 8 EPROM memory. Calculated values of standard deviation were compared with those obtained for the same converter without additional dither and with noise non-subtractive dither, obtained in simple circuit shown in Fig. 3a.

Calculated values of standard deviation and effective resolution for low values of input signal are given in Fig. 5 and in Table 1. It was established, that for high-resolution A/D converters, effectiveness of non-subtractive dithering is limited, and optimum amplitude of the noise dither signal is very low (ca 6μV in our case. Dithering with self-subtractive, deterministic dither signal, was more effective for elimination of unwanted peaks of errors, observed near zero values of input signals. Amplitude of self-subtractive dither signal is less critical and in our case optimal value is about 20 μV. With self-subtractive dithering Increase in effective resolution was from 1.5 bits for the longest averaging period of output filter-decimator up to 4 bits (16 LSB) for the shortest averaging time.

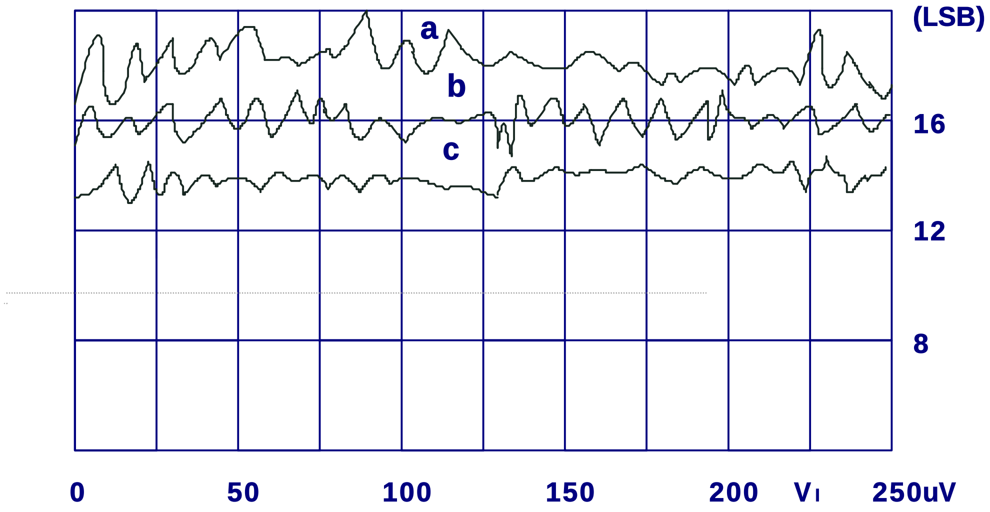

Fig.6. The effective values of conversion errors
in nominally 24-bit sigma-delta A/D converter for low-value DC inputs.
a - with 6μV non-subtractive noise dither,
b - with 6μV self-subtractive deterministic dither,
c - with 20μV self-subtractive deterministic dither

Table 1. The worst case values of the effective resolution
of nominally 24 bit sigma-delta A/D converter without and with dithering

First pole of output filter- decimator	Effective resolution (bits) without dithering	Effective resolution (bits) with non-subtractive stochastic dithering	Effective resolution (bits) with self-subtractive deterministic dithering
10 Hz	21,5	22,0	23,0
100 Hz	19,5	21,0	22,0
1000 Hz	17,5	20,5	21,5

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