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ULTRAHIGH SPEED SAMPLE AND HOLD DYNAMIC CHARACTERIZATION WITH A 12 BITS ACCURATE ADC.

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Abstract: this paper reports the main dynamic tests results about two (2)main ultrahigh speed Sample and Hold (S/H). For the different testing analyses, the laboratory used the well-known 14bits Analog to Digital Converter (ADC) ADC614KH (14bits/5.12MHz) .This ADC is manufactured par the US BURR-BROWN company . The two evaluated S/H are available on the commercial market . These are the S/H AD9100JD (US ANALOG DEVICES company) and the SHM12S (US DATEL company).
Keywords: Dynamic tests results, ultrahigh speed Sample and Hold, testing analyses

1 MAIN IDEAS

The technical choice of an ultrahigh speed S/H is not easy. If the Acquisition Time (Tacq from the HOLD to TRACK mode) is considered like the most critical dynamic parameter which reduces drastically the accuracy of an S/H, the Droop Rate is also an other parameter (HOLD mode) which helps the user to a conditioning signal choice design. To assess the behavior of these two critical dynamic parameters, we connected the output S/H under test to the core of the ADC614. Before doing that, we cut the internal ADC614 connection line between the output S/H and the input conversion stage. First of all, the ADC is tested like a 'stand-alone' 12 bits converter. All the ADC614 dynamic parameters we measured constitute the basic measurements database of our testing method. The assessment of the all unknown S/H spectral parameters (connected to the ADC614 core) will be do by the Tacq modulation (HOLD to TRACK mode). Then we'll evaluate the behavior of the S/H when the 'δt HOLD time' is modulated . Explanation: the 'δt HOLD time' is the delay between the S/H TRACK to HOLD mode and the Start Convert trigger of the ADC core. By a Tacq fixed value, the Droop Rate phenomena will be analyze. Finally, we'll explain the different applications capabilities of these S/H through an asynchronous analog Sampling acquisition system. The laboratory has evaluated two (2) of the main ultrahigh speed S/H COTS .

2 ADC614 SCHEMATIC FUNCTION

The BURR-BROWN ADC614 is a two step hybrid 'sub-ranging' converter with a S/H stage in front of the conversion core. Note that the S/H output ,internally connected to the ADC core, is useable by the user. This particularity is the main reason about the our ADC product choice. In this way, the ADC core consists of the main element of the dynamic testing method. Furthermore, we selected the ADC614 because it's a very high accurate ADC which the input analog amplitude (±1,25V) is compatible with the input amplitude signal of the S/H (±1V) to be tested. Finally, the testing ADC614 configuration was a 12 bits resolution because our first test system (DAS 9229 TEKTRONIX) didn't permit the upper resolution testing.

2.1 Internal functional timing of the ADC614

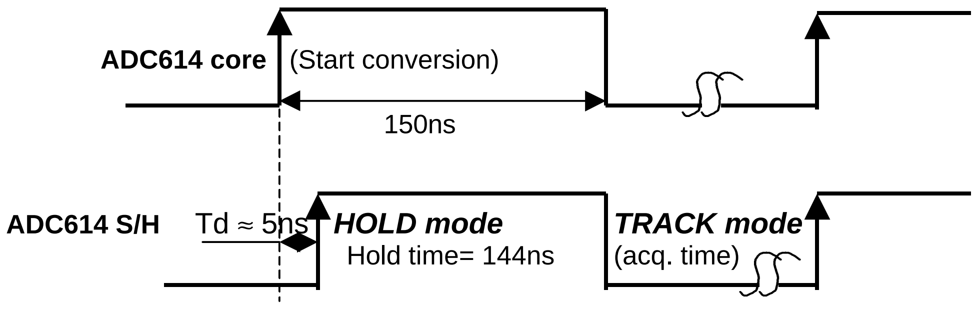
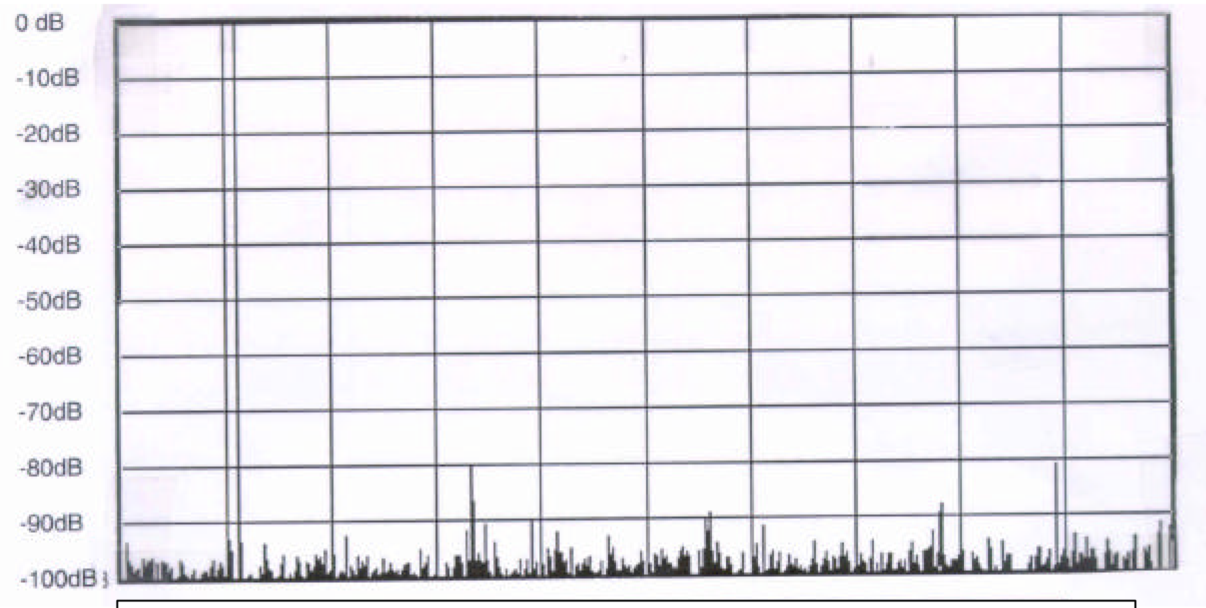


Figure 1: internal ADC614 functional timing

remark : the internal timing management indicates that the HOLD time is fixed to 144ns. Only the Acquisition Time (Tacq) depends from the Sampling Frequency Fs . In this case, if Fs=5.12MHz, Tacq=(1/Fs –144)=51ns. When the Start Convert effectively begins, the S/H changes from the TRACK to HOLD mode 5ns later.

2.2 ADC614 referenced Dynamic spectral tests :

To prepare the unknown S/H spectral dynamic testing evaluation which dépends from the modulated acquisition time (Tacq), we selected the testing NYQUIST frequency couple like Fs=4MHz and Fin≈1,995MHz. Keep in mind that if Fin≈ Fs/2, the S/H should have success to acquire all the input analog signal during the TRACK mode. Finally, the ADC614 is tested like a 12bits ‘stand-alone’ converter.



SINAD=68dB ENOB=11bits SNR=68,28dB THD=79,9dB SFDR=80,13dBc

Figure 2: ADC614 spectrum when Fs=4MHz and Fin=1.995MHz

To evaluate the spectral dynamic S/H parameters which depend from the ‘δt Hold Time’ before the effective trigger ‘Start Conversion’ of the ADC614 core, we have selected the testing NYQUIST frequency couple : Fs=10kHz (T=100µs) and Fin≈ 4,98kHz. All the dynamic measurements values obtained at these low frequency conditions will be more accurate than the values obtained when Fs=4MHz.

3 S/H TEST BENCH EVALUATION:

The evaluation success about the two studied dynamic mode behavior of the S/H under test either depends of the timing management clock of the S/H and the ADC614 core. Now, the internal ADC614 S/H output is disconnected from the ADC614 encode core (the internal connection is really broken). So, to manage the timing clocks, some signal generators must be used. Note that the input analog signal is band-pass filtered.

3.1. Test bench schematic

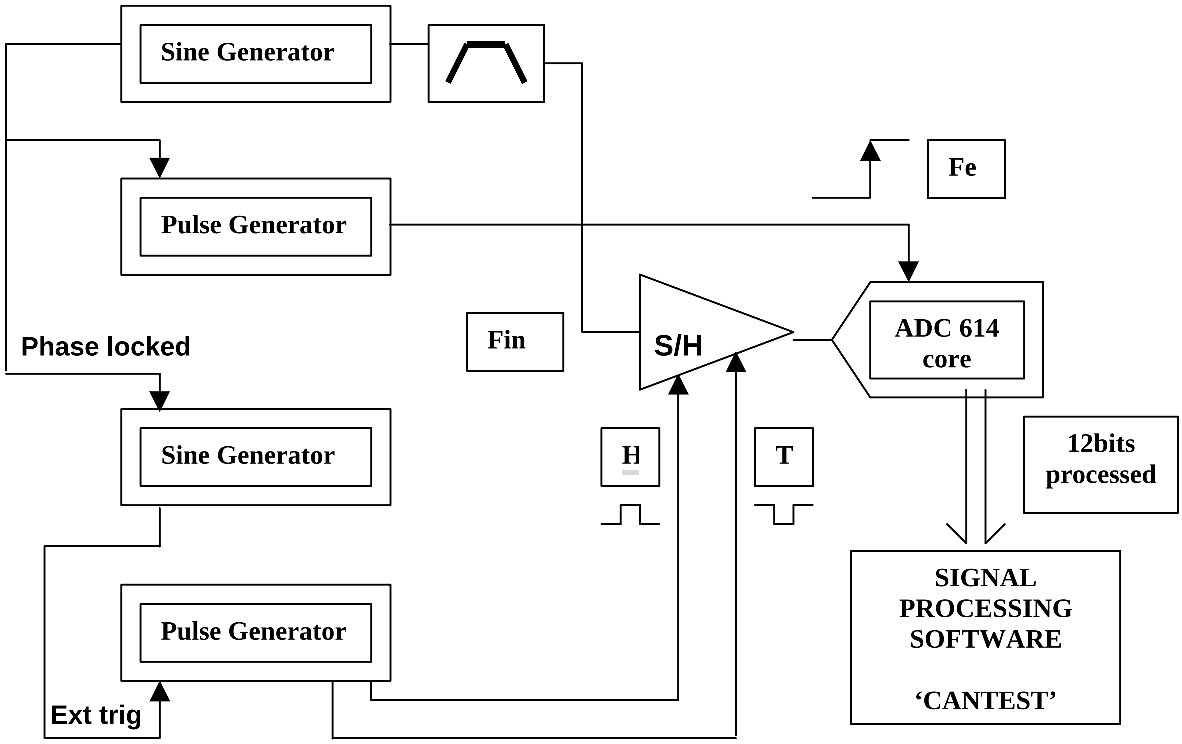


Figure 3: schematic test bench description

3.2 Dynamic S/H measurements by acquisition time Tacq modulation :

3.2.1 Testing principle

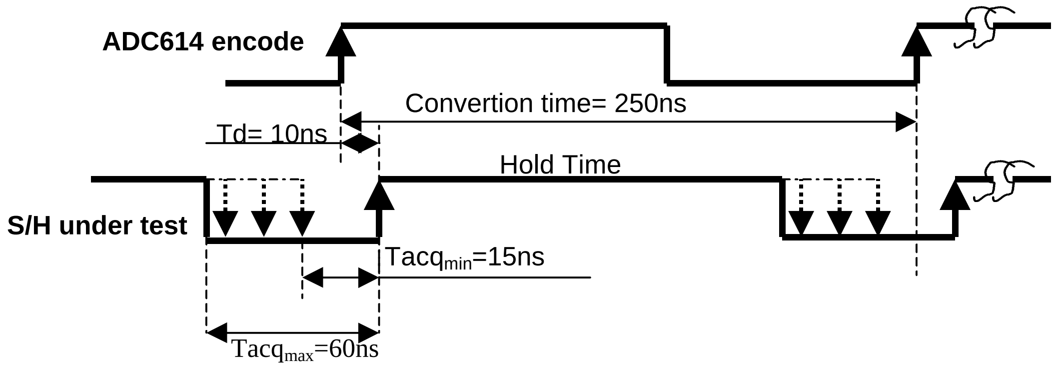


Figure 4 : timing management

special testing conditions:
• concerning the S/H SHM12S (DATEL product), the user has the possibility to add an external Hold capacitor $C_{hold.}$ We did it by adding a 47pf external C_{hold} capacitor. The load resistor R_{load} is fixed to 1kΩ.
• concerning the S/H AD9100 (ANALOG DEVICES product), it's not possible for the user to add an external Hold capacitor. In fact, the C_{hold} capacitor is internally defined. In this case we only selected the load resistor R_{load}=1kΩ .
Based on these defined tests configurations, the either spectrum S/H FFT are recorded when the Tacq is modulated from 15ns up to 60ns.

3.2.2 results:

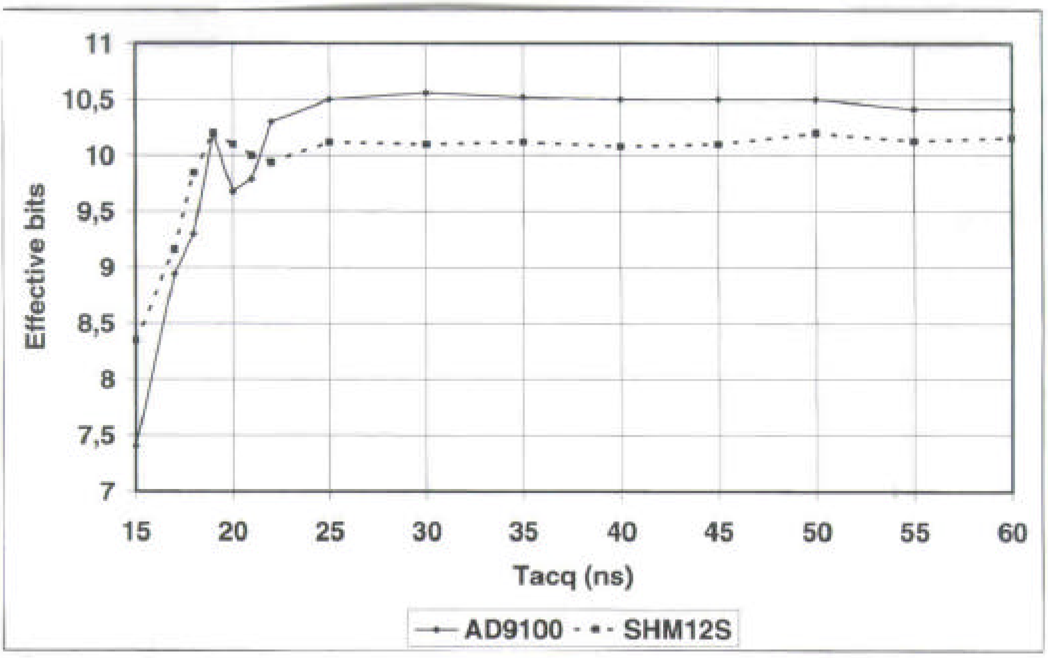


Figure 5 : accuracy ENOB curves versus Tacq

some remarks:

1. whatever S/H is tested, the maximum accuracy we measured is around 10,5 effective bits. So, this result is less accurate than the basic database internal S/H measurements of the ADC614.
2. The AD9100 S/H is more accurate than the DATEL S/H by a value around 0,4 effective bits when Tacq ≥ 25ns. This delta ENOB accuracy between the two S/H is essentially due to the THD spectral parameters. SNR spectral parameters results are near the same.

Concerning the two S/H under test, these are the main spectral dynamic parameters measured when Tacq=18ns and Tacq=60ns.

	Tacq= 18ns					Tacq= 60ns				
S/H	**SINAD (dB)**	**ENOB (bits)**	**SNR (dB)**	**THD (dB)**	**SFDR (dBc)**	**SINAD (dB)**	**ENOB (bits)**	**SNR (dB)**	**THD (dB)**	**SFDR (dBc)**
AD9100	57,68	9,29	65,54	58,46	59,08	64,49	10,42	64,54	84,58	84,07
SHM12	61,12	9,86	65,23	63,26	64 ,34	62,94	10,16	64,45	68,26	68,28

Table 1 : the two S/H spectral parameters

3.3 Dynamic S/H measurements by 'δt Hold Time' modulation :

3.3.1 Main testing idea:

3.3.2

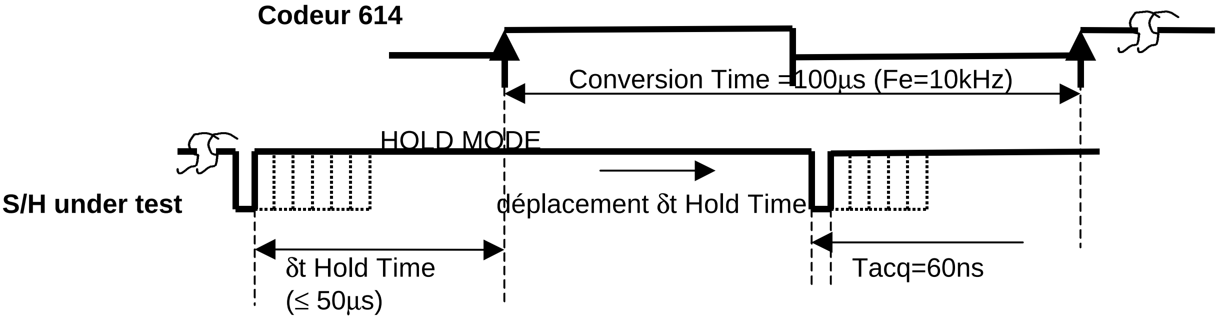


Figure 6: timing management

In this case, we are going to evaluate the S/H dynamic spectral parameters when the Hold Time, before the effective beginning Start conversion of the ADC614 encode core, is modulated up to 50 µs. We called this time delay , the 'δt Hold Time'. The Tacq will be fixed to 60ns. The external C_{hold} and R_{load} are the same that the previous test. The Droop Rate phenomena (the droop helded analog signal) will be explain on graphics.

3.3.3 results:

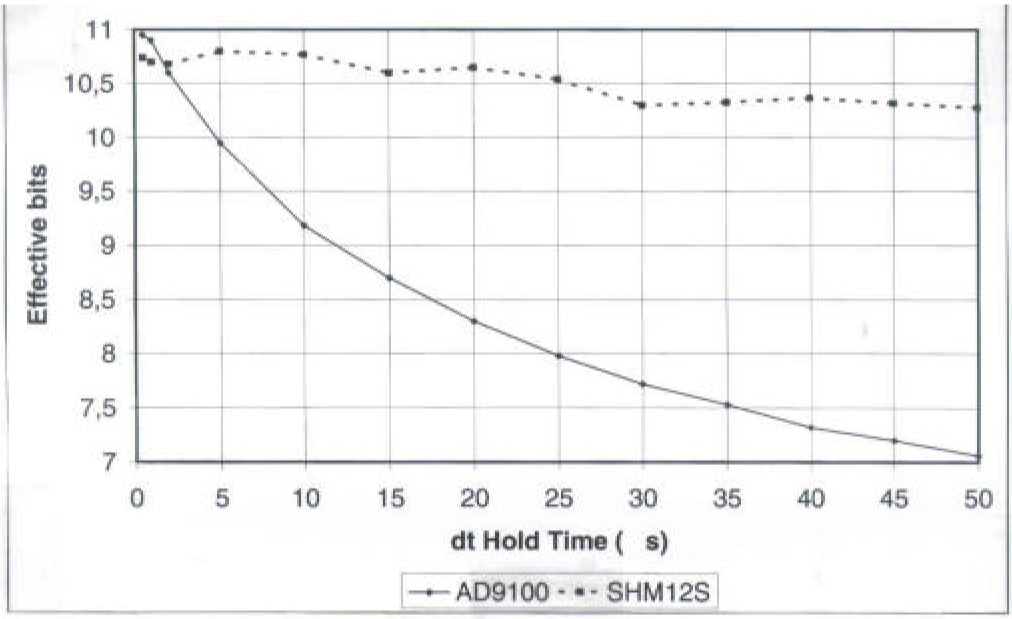


Figure 7 : accuracy ENOB curves versus 'dt HoldTime' when Tacq=60ns

remarks:

1. whatever the 'δt Hold Time' tested about the S/H SHM12S (DATEL product), the accuracy is over 10.2 effective bits ($ENOB_{max}$ < 10.7bits). That demonstrates the droop of the helded analog signal is small and the Droop Rate is staying pseudo-linear up to 50µs 'δt Hold Time'. In an other hand, the accuracy of the S/H AD9100 dropped very quickly when 'δt Hold Time' > 2µs.
2. By seeing the dynamic behavior of the two S/H when 'δt Hold Time' is modulated, we conclude that the SHM12S (DATEL product) is more accurate than the AD9100 (ANALOG DEVICES product).

Concerning the S/H under test, these are the main spectral dynamic parameters when 'δt Hold Time'= 10µs ; furthermore Tacq=18ns and Tacq=60ns.

	Tacq= 18ns					Tacq= 60ns				
S/H	SINAD (dB)	ENOB (bits)	SNR (dB)	THD (dB)	SFDR (dBc)	SINAD (dB)	ENOB (bits)	SNR (dB)	THD (dB)	SFDR (dBc)
AD9100	56,97	9,17	57,43	66,89	68,24	57,04	9,18	57,10	75,39	73,85
SHM12	62,32	10,06	68,36	63,56	66,73	66,6	10,77	68,48	71,16	71,24

Table 2 : the two S/H spectral parameters

3.4 Dynamic Evaluations analyses:

The dynamic parameters evaluation have been measured about two different design S/H. At the first time, the acquisition time (Tacq) was modulated and after that the 'δt Hold Time' was modulated .These two technical tests methods permit to distinguish two main critical points:

- By modulating the Tacq, (Thold < 235ns), we can see that either ultrahigh speed S/H indicates a constant accuracy when Tacq ≥25ns. Furthermore, the AD9100 S/H is more accurate than the SHM12S S/H.
- By modulating the 'δt Hold Time', we can see that the behavior of the two S/H is completely different each other. In fact, whatever 'δt Hold Time' ≤ 50µs , the SHM12S S/H accuracy is over 10.2 effective bits. In an other hand, the AD9100 S/H accuracy dropped very quickly when 'δt Hold Time' > 2µs.

Now it's possible to extract some technical benefits from the all previous dynamic analyses about the ultrahigh speed SHM12S S/H. Keep in mind this device is able to combine a very quick acquisition time and an accurate helded analog signal (pseudo-linear Droop Rate up to 50µs). So, one of the typical application could be to incorporate this S/H DATEL product into an multiple channels acquisition system design based on the asynchronous high sampling rate principle.

3.4.1 Multiple channel asynchronous sampling acquisition system :

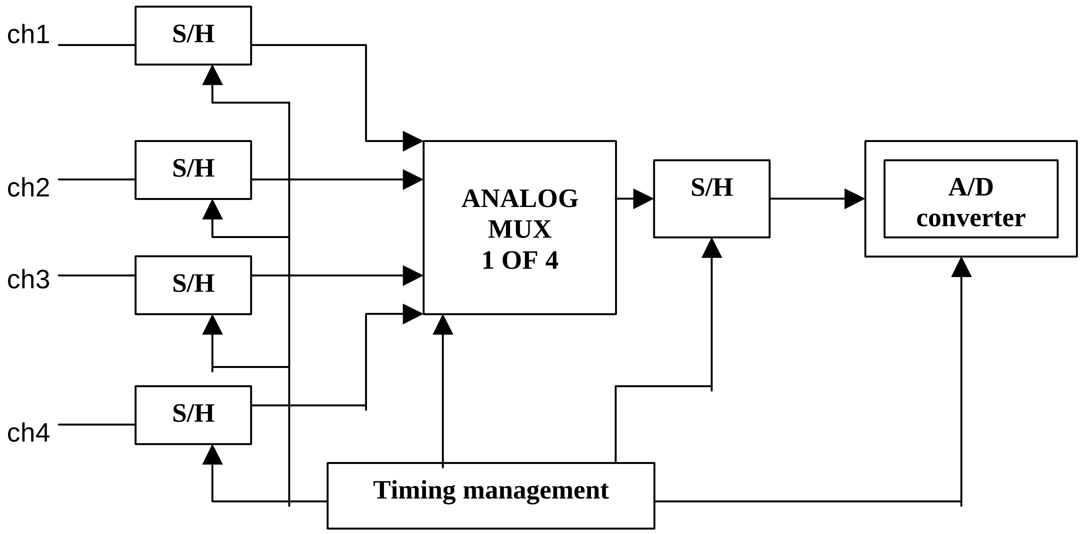


Figure 8 : schematic multi-channel architecture designed with n S/H and one (1) ADC

The main interest of such a system is the possibility to acquire some repetitive or single signals and to hold the sampled analog signal up to 50µs with a great accuracy. Then these signals are multiplexed through an analog multiplexer. Finally, an other S/H (or not) implemented at the output of the multiplexer can sampled the helded output analog signal. Then the A/D stage convert the 'helded' signal. By keeping the same technical possibilities, this acquisition system (n S/H with only one A/D converter) is able to replace the same number of S/H (different from the SHM12S) which would be each followed by one A/D converter. The new solution (SHM12S incorporated) permits to reduce the power consumption and the cost.

4 CONCLUSIONS:

The CELAR 'Signal processing' laboratory lead a comparative technical analysis about two ultrahigh speed S/H . These analog products can be included in a conditioning analog signal system design. If the HOLD to TRACK mode study demonstrated the capability of the S/H to acquire very quickly an analog signal with a specified accuracy, the technical study of the HOLD mode permitted the 'well-knowing' of the S/H capability to hold the analog signal as accurate as possible perhaps during a long delay time. By the well-known behavior about the different functional modes of the S/H, the multiple channels acquisition system design may be sometimes more easy and less expansive.

REFERENCES:

⟨1) 'High Speed Design Seminar Analog Devices 1989 : ANALOG DEVICES'
(2) AD9100 Data Sheet : 'Ultrahigh Speed Monolithic Track-and-Hold' (ANALOG DAVICES)
(3) SHM12 Data Sheet : 'Ulltra-Fast, 12-Bit Linear Monolithic Sample-Hold Amplifiers' (DATEL)
(4) ADC614 Data Sheet : '14-Bit 5.12MHz Sampling ANALOG-TO –DIGITAL CONVERTER' (BURR-BROWN)

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