

HDL-A MODELLING OF SWITCHED-CURRENT DELTA SIGMA A/D CONVERTERS

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Abstract: Switched Current (SI) is a very interesting analog technique to perform interface circuits in mixed analog/digital systems because it is compatible with a low cost digital CMOS process (single poly technologies). The attempt of this work is to shed some light on the SI delta-sigma converter design method making use of an analog Hardware Description Language. To demonstrate the performances of the HDL-A model to optimize delta-sigma converters, a first order SI delta-sigma modulator has been designed, simulated and implemented using a 0.7 μ m CMOS digital process. Also we have compared the simulated results and the experimental.

Keywords: Switched-Current, Delta-sigma converters, Mixed-signal

1 INTRODUCTION

Switched current (SI) is a very interesting design method to perform interface circuits in mixed analog-digital systems because it is compatible with a standard digital CMOS process (single poly technologies) [1]. The implementation of high performance SI cells (current copier cells, integrators, delta-sigma modulators, etc.) requires an accurate design procedure, which considers the relation between the expected cell characteristics and the technological and layout parameters. The SI non-idealities such as the mismatch, the settling time during acquisition, the clock-feedthrough error and the effect of the variation of the output conductance with the signal level are the origin of the harmonic distortion observed in SI circuits [2,3].

Making use of an analog HDL we can model not only analog components but also digital. Working in this way we can make an integrated model including analog and digital parts of the converter. It is not possible to make this complete model with HSPICE which we can only work at transistor level with. Otherwise, HDL-A have some features that make it suitable to design data acquisition systems as his ability of model non-electrical subsystems. So mechanical, thermal, rotational, fluidic and others kind of variables can be implemented. In this sense, a complete microsystem including sensors, transducers and their interface circuits can be simulated.

In this framework, the paper is organized as follows: in section 2. a complete current-mode analog to digital converter is described, section 3 explains the simulation procedure using HDL-A, experimental results for the complete A/D converter as well as the comparison between these and simulation results will be shown in section 4. Finally, in section 5 the main conclusions are reported.

2 CURRENT MODE A/D CONVERTER

Our attempt is to obtain a direct method to model and to implement the Switched Current based analog to digital converter. To demonstrate the performances of the HDL-A model to optimize delta-sigma converters, a first order SI Delta-sigma modulator (Fig. 1), has been designed, simulated and implemented using a 0.7 μ m CMOS digital process from Atmel-ES2.

The architecture of the Delta-Sigma converter chosen has been a fully differential first order modulator (Fig 1). The main non-idealities of the modulator appear on the differential integrator as well as on the comparator. For an easier understanding of the ideal and non-ideal behaviour of the switched-current circuits, we will report first, the simplest SI memory cell (Fig. 2).

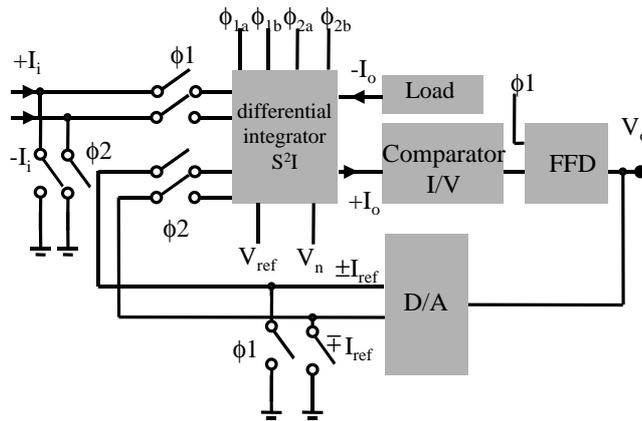


Figure 1: Full differential first order sigma-delta modulator

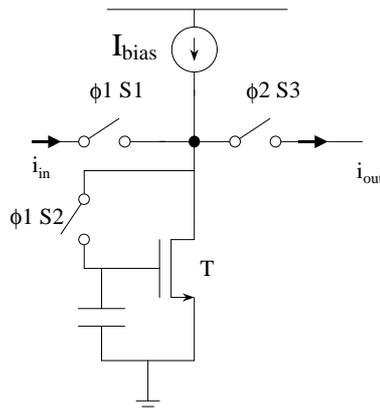


Figure 2: Basic switch current memory cell (SI)

In the basic SI cell depicted in Figure 2 the same transistor works as input or output device, depending on the clock phase. So, during clock phase f_1 , the switches S1 and S2 are closed and in consequence the diode-connected transistor generates the gate voltage corresponding to the input current i_{in} , plus the bias current I_{bias} , (the transistor is in its saturation region, so the relationship between current and voltage is a square-law). During the second phase f_2 , switches S1 and S2 are open, while MOS switch S3 connects the transistor drain to the output load.

A reduction of the clock feedthrough effect and an increase of the sampling frequency is obtained using a modified SI cell, known as S^2I cell (Figure 3). An improvement of the cell behaviour is obtained by substituting each transistor for a cascode stage. All the modules designed in this interface are based on S^2I cascode memory cells.

Figure 4, corresponds to a simplified full-differential SI integrator, which has the same functionality as the obtained in our design changing each cell for a S^2I cascode cell. One of the main drawbacks of this schema is that it is necessary to remove the common mode signal. We have used a system based on the common mode feed forward [3,4].

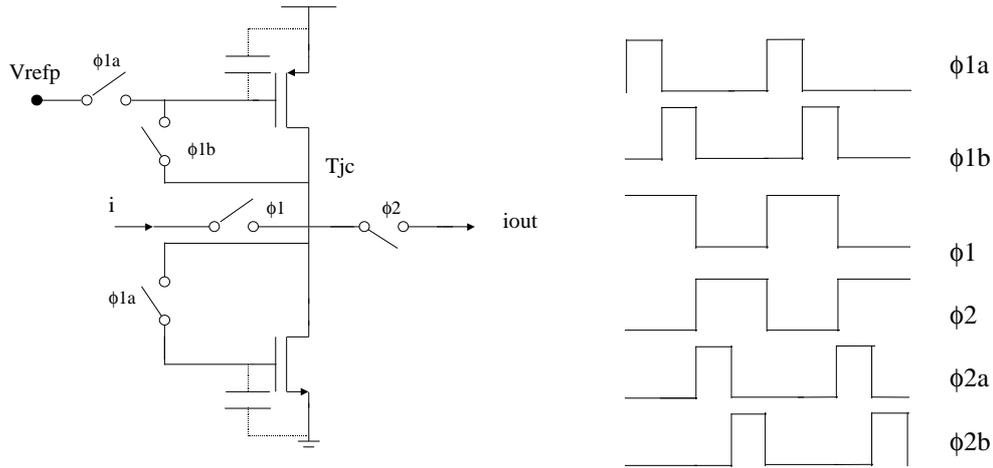


Figure 3: A) Basic S^2I memory cell. B) Clock schema used

The comparator schema is shown in figure 5. It is based on a current-voltage converter which main feature is a low input impedance. Finally the 1 bit D/A converter module (figure 6) can be implemented as a current source controlled by the comparator output voltage.

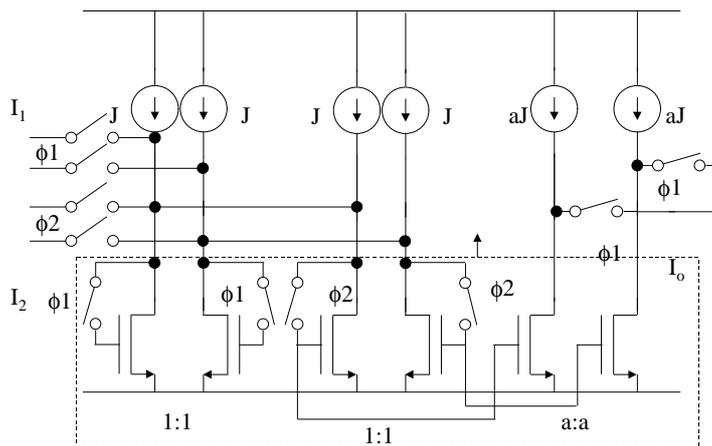


Figure 4: Full differential SI Integrator

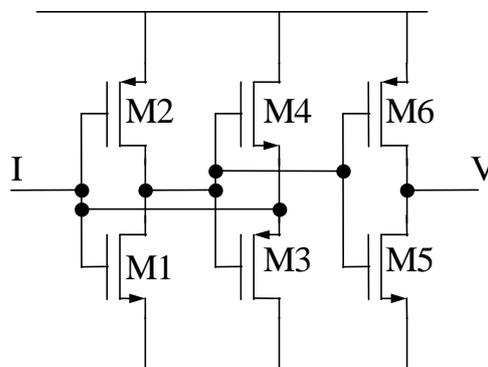


Figure 5: Current voltage comparator

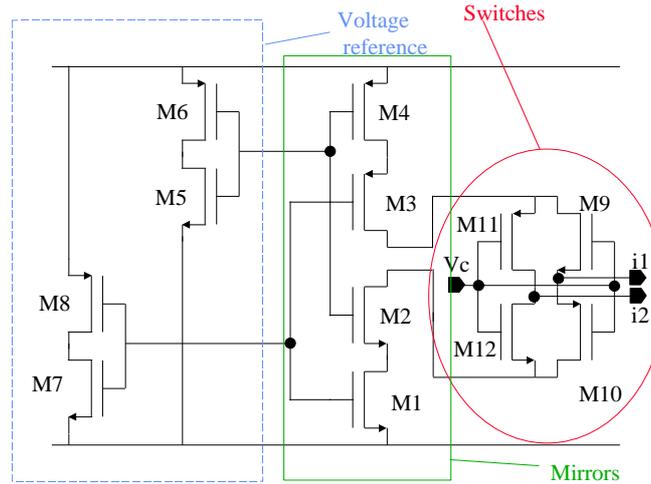


Figure 6: 1bit D/A Converter

3 HDL-A MODELING

It is clear that the analysis of the $\Sigma\Delta$ modulator at transistor level made with an electrical simulator under normal operating conditions, requires an excessive computing time. To reach the goal of complete simulation of the system, it is necessary to build a macromodel of the basic S^2I memory cell, including the non-ideal effects. This model allows a quick (short computing time) and accurate simulation of the cell characteristics and its straightforward application to more complex SI circuits, which includes several memory cells. In order to model the A/D converter we have to consider some important aspects related to the switched currents circuits. Previous works have pointed out the influence of the mismatch, the settling time during acquisition and the capacitive coupling errors in the non-ideal characteristics of basic SI cells [5-8]. Moreover, the clock feedthrough error, which is inherent to the use of switches, is another important drawback in SI design. All these effects together with the variation of the output conductance with the signal level and the error in the input voltage/current conversion will contribute to the harmonic distortion observed in SI circuits.

For an HDL-A description it is necessary to write down the equations describing the behavior of every individual block. Analytical rather than numerical relations are preferred in order to have explicit dependence on physical and design parameters. In some cases, when it is not possible to obtain analytical expressions because of the existence of strongly non-linear responses (for instance a comparator behavior), the component can be modeled in the form of a fitted expression from results obtained by simulation at physical level. Both procedures, analytical and fitted, has been applied to the different modules of the system and in the next part of this section we will illustrate the relevant points of them with the examples corresponding to the integrator and the comparator.

To perform the HDL-A model of the S^2I integrator, we have considered the current behaviour of the transistors as a function of the gate-source voltage and drain-source voltage in the saturation region

$$I_D = \frac{mC_{ox}}{2} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{ds}) \quad (1)$$

$$V_{ds} \geq V_{gs} - V_T$$

where I_D is the drain current, m the carriers mobility, C_{ox} the oxide capacitance, W and L the width and the length of the channel respectively, V_T the threshold voltage, and V_{gs} and V_{ds} the gate-source and the drain-source voltage respectively.

To include the clock-feedthrough effect the V_{gs} value of each transistor is modified by a value ΔV_{gs} according.

$$Q_{ol} = C_{ol} (V_H - V_L) \quad (2)$$

$$Q_{ch} = C_{ch} (V_H - V_{gs} - V_T) \quad (3)$$

$$\Delta V_{gs} = \frac{Q_{ol} + \alpha Q_{ch}}{C} \quad (4)$$

Where, α is a factor of the channel charge stored in the capacitor of the memory cell.

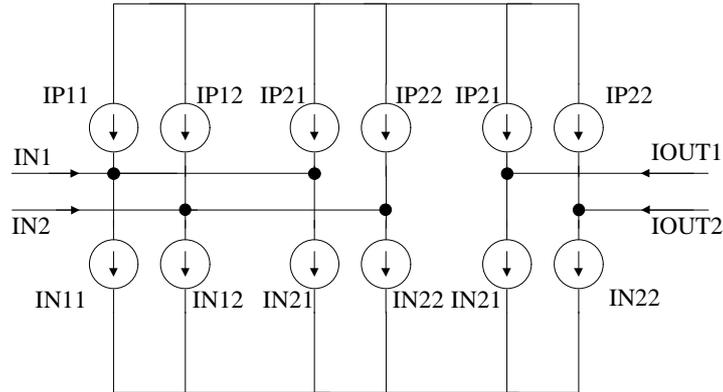


Figure 7: Schema of integrator model in the HDL-A simulation

Considering Kirchow Laws and the simplified schema of figure 7 it results:

$$\begin{aligned} IP11 - IN11 + IP21 - IN21 + IN1 &= 0 \\ IP12 - IN12 + IP22 - IN22 + IN2 &= 0 \\ IOUT1 &= IP21 - IN21 \\ IOUT2 &= IP22 - IN22 \end{aligned}$$

Taking into account that our integrator is controlled by the phases shown in the figure 3B, it is necessary an equations system description of all currents for each clock phase, considering :

- For every clock phase the input node voltage corresponds to a principal transistor voltage.
- In every phase is one transistor diode-connected while the others fix their currents

For instance we can write, for each input and using the notation (n) for the clock period, $I_{XX}(n)$ the value of the current I_{XX} at the end of clock phase, and J as the bias current of the memory cell.

Phase Φ_{1A} ON

$$\begin{aligned} IP1[n] &= J \\ IP2[n] &= IP2[n-1/4] \\ IN2[n] &= IN2[n-1/4] \\ IN1[n] &= IIN[n] + J + IOUT[n-1/4] \end{aligned}$$

Phase Φ_{1B} ON

$$IP1[n+1/4] = IN1[n] - IIN[n+1/4] - IOUT[n-1/4]$$

The other currents not change

Phase Φ_{2A} ON

$$\begin{aligned} IP1[n+2/4] &= IP1[n+1/4] \\ IN1[n+2/4] &= IN12[n] \\ IP2[n+2/4] &= J \\ IN2[n+2/4] &= J + IIN2[n+2/4] + IP1[n+1/4] - IN1[n] \end{aligned}$$

Phase Φ_{2BON}

$$IP2[n+3/4]=IN1[n+3/4]+IN2[n+3/4]-IIN2[n+3/4]-IP1[n+3/4]$$

The other currents not change

The combination of these equations, allows to obtain the Z-transfer function.

$$IOUT(z) = \frac{z^{-1}}{1-z^{-1}} IIN1(z) - \frac{z^{-1/2}}{1-z^{-1}} IIN2(z) \tag{5}$$

We remark that it is necessary to introduce a phase shift to obtain the integrator transfer function, obtained using a D flip-flop. In the case of the comparator module, the model included in the HDL-A description has been performed using polynomial fitting of the SPICE analysis (Figure 8) considering three different regions, (from $-\infty$ to $0^- \mu A$, from 0^- to $0^+ \mu A$, and from 0^+ to $+\infty \mu A$) and imposing continuity between them.

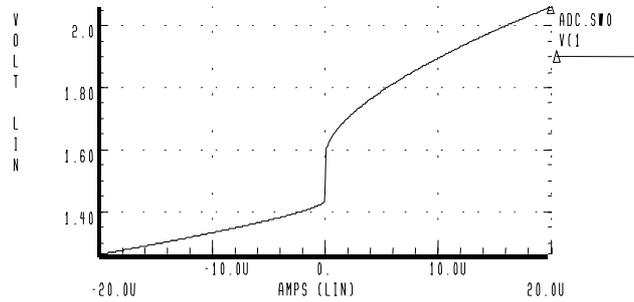


Figure 8: SPICE simulation of the comparator showed in figure 5

4 RESULTS

In order to test our HDL-A model for the first-order current-mode sigma-delta modulator, and to compare with SPICE and experimental results, we have used the same conditions about the input levels and the clock frequency being both 10 mA and 1.024 MHz respectively.

The merit figure to study will be the signal-to-noise ratio plus distortion because of the direct relationship between it and the resolution of the digital output in $\Sigma\Delta$ A/D converters.

We present in figure 9. the HDL-A curves (both, ideal and non-ideal) as well as the experimental one. It can be observed a good agreement between HDL-A and experimental results (less than 3dB of deviation) which confirms our analysis.

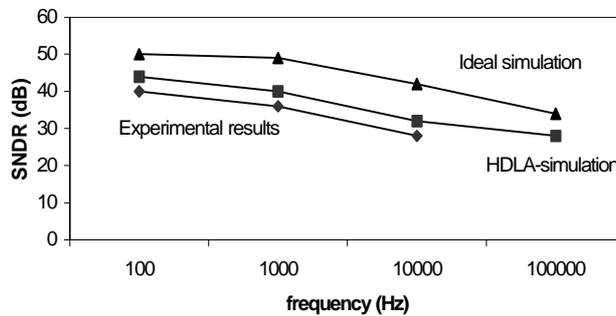


Fig 9: Signal to Noise plus Distortion ratio of the complete microsystem

5 CONCLUSIONS

The concept of a current-mode system with digital output, based on the previous blocks and a specific first order current-mode delta-sigma converter is presented. There is a good agreement between the experimental results of the converter compared with the simulation results of the HDL-A models. So, these modelling methods are expected to make a good A/D delta-sigma SI converter design method.

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