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TESTING INL OR DNL—IS THERE A TRADE-OFF?

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Abstract: Traditionally, production testing of data converters is based on measuring either the Integral or the Differential Nonlinearity (INL or DNL), respectively and computing the other. Doubts about this practice are raised as examples show that some error mechanisms in a given circuit have a characteristic INL-signature while others have a distinctive DNL-signature.

In this work we address the question "should one measure INL or DNL." We extend the Linear Error Mechanism Modeling Algorithm [15] to use both INL and DNL measurements simultaneously (if so required) to measure a device under test (DUT) with maximum accuracy given a fixed number of measurement points.

Keywords: Integral and Differential Nonlinearity, Mixed-Signal test

1 INTRODUCTION

Analog-to-Digital Converters (ADCs) are commonly tested for INL and DNL specifications using the histogram method [1, 2, 3]. Using this method, the DNL characteristic versus code is measured and the INL is computed from this as the cumulative sum. In [4] it is shown that the test time quadruples with every additional bit of resolution for the converter under test if we want to keep the relative accuracy of the computed INL constant, at say 0.1 LSB. As an alternative to the histogram method, the servo-loop method [5] can be used to measure the transition levels and hence the INL of an ADC. Using a model-based testing approach, we can reduce the number of transition level measurements to a minimum [6, 7] and possibly outperform the histogram method in terms of test time [8, 4].

Besides long test times, we observe that (depending on the architecture of the converter circuit) a parameter which deviates from its designed value exhibits a characteristic signature in the INL or DNL versus code characteristic. Approaches to model-based testing (which have long been recommended for minimizing test effort [9]) estimate the circuit parameters of the device under test (DUT) from a reduced set of response measurements and then use the model to predict the full device response and, in particular, to identify where it fails to meet the specifications.

Estimating the model parameters accurately for each individual DUT is critical; for parameters that have a characteristic INL signature, we should henceforth perform INL measurements, and for others we should perform DNL measurements. Moreover, the modeling approach should use DNL and INL information to build a model that incorporates both of these aspects of the transfer function of a converter. In this work, we propose two things: a way to build a mixed INL/DNL model, and a way to use INL and DNL measurements on the production line.

The paper is organized as follows: Sec. 2 presents a measurement setup for ADCs that allows us to measure INL and DNL at any given code c. In Sec. 3, we outline the steps in modeling the static response of an ADC. Here we also introduce the concept of merging INL and DNL modeling information to obtain a hybrid model. In Sec. 4, we detail the test point selection procedure. Selecting a reduced subset of the possible 8192 INL and DNL test points is central to the model-based testing approach, as this yields the reduction in production test time [10].

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2 MEASUREMENT SETUP

To measure the upper transition level of an ADC

$$V(c) = \{V_{\rm in} \,:\, P(\text{output code} \leq c) = 0.5\} \tag{1}$$

at an isolated code c, a servo-loop setup has been suggested in [5]. Prediction of the full converter characteristic from transition level measurements at a subset of codes using the servo-loop method and a linear error superposition model has been demonstrated for ADCs in [6] and [7].

The basic servo-loop setup can be extended to measure the difference between two transition levels $V(c_u)$ and $V(c_l)$. Measuring the difference $V(c_u) - V(c_l)$ directly is inherently more accurate and faster than measuring both transition levels separately and computing the difference. In the setup shown in Fig. 1, the device under test (DUT) is continuously converting at its specified rate. The DUT is shared between two servo-loops by switches that are clocked at half the converter's sampling rate. Each loop comprises an integrator, the DUT, and a comparator that controls the polarity of the integrator's input. When both loops have settled to their steady-states (which is a triangular wave at each integrator output) the outputs of the integrators have average voltages equal to the transition levels $V(c_u)$ and $V(c_l)$, respectively.

Provided we choose $c_l = c_u - 1$, using two digital voltmeters (DVM) as shown in the figure, we can measure the

$$\mathrm{INL}(c_u) = \frac{V(c_u)}{V_{\rm LSB}} - c_u \quad \text{and} \tag{2}$$

$$\mathrm{DNL}(c_u) = \frac{V(c_u) - V(c_l)}{V_{\rm LSB}} - 1, \tag{3}$$

where $V_{\rm LSB}$ denotes the average voltage step between two consecutive transition levels.

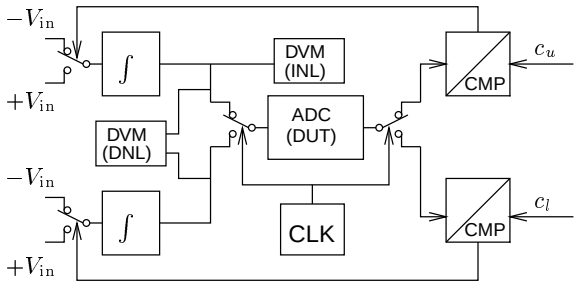

Figure 1: Servo-loop setup, extended to measure INL and DNL of an ADC.

Note that measuring the DNL directly is inherently more accurate than calculating it from two separate INL measurements as would typically be done based on the relationship

$$\mathrm{DNL}(c_u) = \mathrm{INL}(c_u) - \mathrm{INL}(c_u - 1) = \mathrm{INL}(c_u) - \mathrm{INL}(c_l). \tag{4}$$

In the case of a device under test that has a conversion resolution of 12 bits, the resolution of the calculated DNL is only 4 bits when a 16-bit-DVM is used for the two consecutive INL measurements. By contrast, directly measuring the DNL uses the full resolution of the DVM for the DNL result. Moreover, if the production tester has two DVMs that can be used in parallel, we can measure DNL and INL at the same code in the time-span of a single INL-measurement.

Both the INL and DNL versus code must be characterized when testing the static properties of the converter under test. For dynamic testing, however, we also want to set the slew rate of the ADC input signal and the previously output code when taking a transition level measurement [11]. With the suggested setup for measuring transition level $V(c_u)$, the previous code is given by the choice of c_l, and the slew rate of the ADC input signal can be set by choosing the voltage $V_{\rm in}$, the magnitude of the input to the integrators.

This suggests that the extended servo-loop setup show in Fig. 1 is sufficiently flexible to characterize both static and dynamic errors. Also, we have suggested in [4] that the servo-loop setup for testing the INL based on reduced set of codes can outperform the histogram method in terms of test time. Indeed, the performance improvement is greater the higher the resolution of the converter under test.

3 MODELING OF ANALOG-TO-DIGITAL CONVERTERS

The modeling approach for ADCs we follow here is detailed in [7]. The objective is to measure the static INL and DNL of the DUT with minimum effort while ensuring that it meets the specifications.

As a vehicle to demonstrate our approach, we use the AD7864, a 12-bit Successive Approximation ADC which is shown schematically in Fig. 2(a). The three most significant bits of the internal DAC are segmented, and the remaining nine bits are realized in an R-$2R$-ladder, as shown in Fig. 2(b).

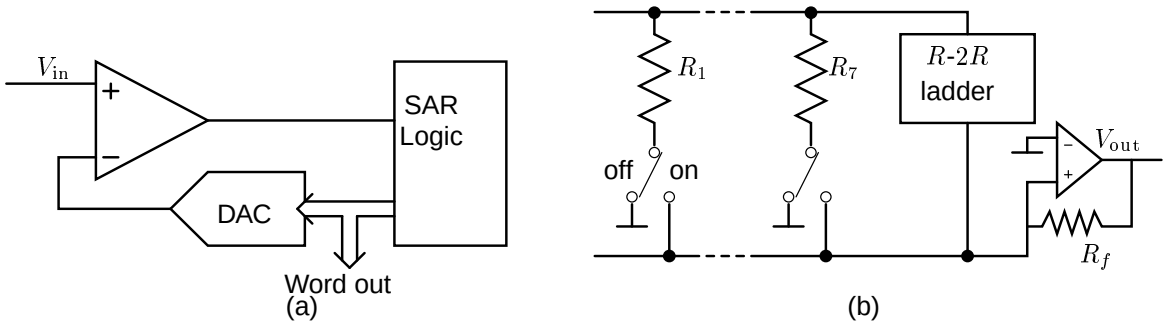

Figure 2: (a) Successive Approximation Register structure, and (b) internal DAC architecture.

To obtain a model for the mechanisms that produce the static INL of the circuit, we perform an analysis of the sensitivity of the INL versus the output code with respect to the circuit parameters. Considering N circuit parameters, for each of them we determine the sensitivity using a circuit simulator such as SPICE [12]. For the example of R_1, we denote by INL_{R_1} the characteristic error $\sigma_{R_1} \cdot \frac{\partial \text{INL}}{\partial R_1}\Big|_{R_1=R_1^0}$, where R_1^0 denotes the nominal value of R_1 and the scalar σ_{R_1} denotes the standard deviation of the spread in the resistor values of R_1 due to the silicon process. For our example, the characteristic INL_{R_1} is shown in Fig. 3.

The underlying assumption of the LEMMA method is that the INL at code c is caused by small circuit parameter variations from nominal. Under this assumption and denoting $\big(R_1 - R_1^0, R_2 - R_2^0, ..., R_N - R_N^0\big)^T$ by ΔR, we consider the Taylor-series expansion

$$\text{INL}(c) = \big(\text{INL}_{R_1}(c), \text{INL}_{R_2}(c), ..., \text{INL}_{R_N}(c)\big)\Delta R + \big(\Delta R\big)^T \left(\sigma_{R_i,R_j} \left.\frac{\partial^2 \text{INL}(c)}{\partial R_i \partial R_j}\right|_{R_{i,j}=R_{i,j}^0}\right) \Delta R + \cdots \quad (5)$$

This expansion is formulated for a circuit comprising a resistor network. Hence the parameters are resistor values R_i. However, we can generalize this to other circuits in which case the parameters are the circuit elements.

In summary, a linear model for the INL characteristic versus code is based on truncating the Taylor series expansion (5) after the linear term. We can then write $\text{INL} = S \cdot \Delta x$, where S is the $m \times N$-sensitivity-matrix of the INL with column j formed by the characteristic INL_{x_j} for the circuit parameter x_j, and each row i represents a code.

Provided that S has full rank (that is given by the number circuit parameters N, provided that $N < m$), then for a device under test it is sufficient to measure the INL at N codes in order to estimate (uniquely) all N elements of the parameter vector Δx. With the estimated parameter vector Δx we can calculate the full INL-response of the device under test using $\text{INL}^* = S\Delta x$. Between the true INL and the calculated (or predicted) INL^*, we expect a discrepancy that we refer to as the "INL-prediction error"

$$e_{\text{INL}}^{\max} = E\Big\{ \max_{\forall c} \big(|\text{INL}(c) - \text{INL}^*(c)|\big) \Big\} \quad \text{or} \quad e_{\text{INL}}^{\text{rms}} = E\left\{ \sqrt{\underset{\forall c}{\text{mean}} \big((\text{INL}(c) - \text{INL}^*(c))^2\big)} \right\}. \quad (6)$$

We can use either the rms- or the max-error here. The maximum prediction error yields a measure for guard-bands that have to be imposed to ensure that the pass/fail decision for a device is not corrupted by the prediction inaccuracies. The rms-error on the other hand yields a measure for how good is the prediction of the general shape of the true characteristic.

For the purposes of estimating the parameters of a device, S is usually not a good choice, especially if S is rank deficient or nearly so. Thus, we replace the sensitivity matrix by an orthogonalized version that we obtain using Singular Value Decomposition (SVD [13]) of $S = U\Sigma V^T$, where S and U share the same range, but U is orthogonal. This new choice of the model matrix implies also a linear mapping to a new parameter space which we reflect in our notation by replacing Δx with Δp.

Note also that the matrix U_n formed by the first n columns of U is orthogonal and has rank n. Based on this observation, choosing a useful model size n can be done by trial and error. For a fixed $n \leq N$, and thus fixed model U_n, we determine e_{INL} for a sample lot of devices. To estimate the parameter vector $\Delta p \in \mathbb{R}^n$ we solve the over-determined linear system of simultaneous equations $\text{INL} \approx U_n \Delta p$ in the least-squares sense and predict $\text{INL}^* = U_n \Delta p$. This yields a graph of e_{INL}, as shown in Fig. 4,

where the dots mark the standard deviation of the e_{INL}. These graphs allows us to trade off model size n versus the accuracy of the model as expressed by the prediction error.

The INL-data used in creating this graph comes from histogram measurements of twenty-four samples of the AD7864 using a triangular input with an average of 64 hits per code [1]. The curve shown as maximum prediction error is dominated more by the measurement noise than by the model inaccuracies, which renders it of little use. By contrast, the rms-error curve is less affected by this noise and allows us to choose n in the range of 16. Choosing $n > 16$ does not yield any further improvement in prediction error.

The technique outlined above can be applied not only to modeling the INL, but also the DNL of a data converter. In the latter case we require for every parameter the sensitivity of the DNL versus code. Due to the special relationship (4) between the INL and DNL, we can "translate" any sensitivity vector previously obtained for the INL into one for the DNL. Thus we obtain from the matrix S, which we now re-name S_{INL}, the sensitivity of the DNL with respect to the **same** set of parameters x. This allows us to extend our former modeling equation $\mathrm{INL} = S\Delta x$ to

$$\begin{bmatrix} (1-\alpha)\mathrm{INL} \\ \alpha \mathrm{DNL} \end{bmatrix} = \begin{bmatrix} (1-\alpha)S_{\mathrm{INL}} \\ \alpha S_{\mathrm{DNL}} \end{bmatrix} \cdot \Delta x$$

which retains the same structure as before with $\alpha \in [0,1]$. Clearly, for $\alpha = 0$ we have a pure INL model, and for $\alpha = 1$ a pure DNL model. In the remainder of this paper we will investigate how the performance of the model changes in terms of prediction error as we vary α.

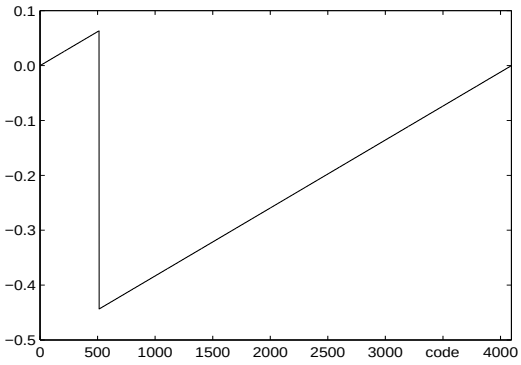

Figure 3: Scaled INL sensitivity for circuit element R_1.

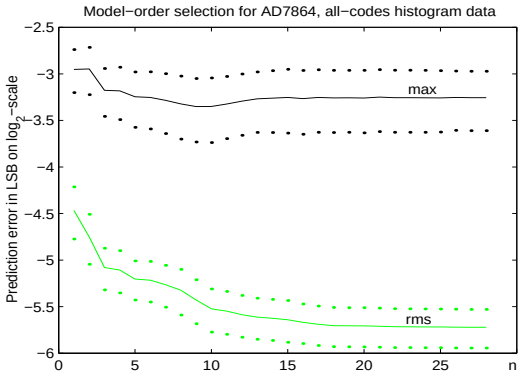

Figure 4: Maximum and rms-prediction error on $\log_2$-scale using all-codes histogram data of 24 sample devices.

4 TEST POINT SELECTION

Instead of measuring all test points of the device characteristic (which could be the INL and/or DNL as shown in the previous section) we aim to select a subset of test codes (i.e. testpoints) at which we measure INL and/or DNL.

In [14], the QR-decomposition of the transpose of the model matrix U_n is performed and the pivots chosen during this decomposition are used as a selection of "maximally linearly independent" rows of U_n. Note that each row of U corresponds uniquely to an INL or DNL test point.

In Fig. 5, we show for our example circuit the graph of $e^{\mathrm{rms}} := \sqrt{(e^{\mathrm{rms}}_{\mathrm{INL}})^2 + (e^{\mathrm{rms}}_{\mathrm{DNL}})^2}$ over the n-α-plane with $\alpha \in [0,1]$ and $1 \le n \le N = 28$. The sample set of 50 devices has been "produced" by SPICE simulations varying the resistor values by 0.1% around their nominal values using a Gaussian distribution. The INL and DNL information created in this way is virtually noise-free. In practice the INL and DNL could only be approximated by highly accurate transition level measurements for a sample set of devices.

To simulate the measurement of the INL and DNL data on the production line, we add Gaussian noise of 2^{-4} LSB to the INL and 2^{-8} LSB to the DNL. These numbers are chosen based on our earlier discussion in Sec. 2 of the measurement setup that enables significantly greater measurement accuracy for the DNL than for the INL.[1]

[1]Currently, the servo-loop setup is under construction, and no data for the AD7864 are available yet. The histogram data which

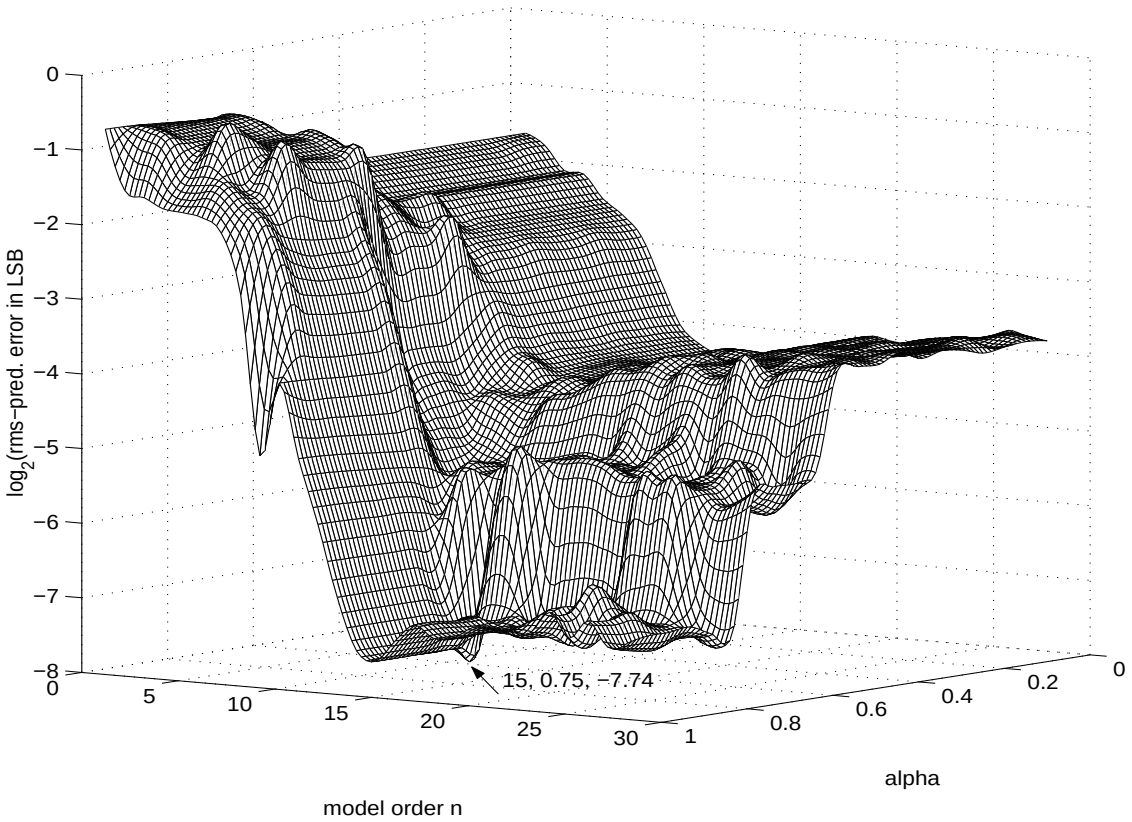

Figure 5: rms-prediction error $\log_2(e^{\mathrm{rms}})$ over n-α-plane using SPICE simulated INL and DNL data.

The graph in Fig. 5 shows that the pure DNL model ($\alpha = 1$) produces more accurate predictions (for $n \geq 10$) than the INL model ($\alpha = 0$). Note that this observation depends on the converter architecture and on the ratio of the noise powers corrupting the INL and DNL measurements used to estimate the model parameters. Nevertheless, producing this graph is a matter of minutes; thus for a given measurement setup and circuit under test we can (based on this graph) optimally choose the parameter α and the model order n.

The minimum of the rms-prediction error is reached for $n = 15$ and $\alpha = 0.75$. The INL and DNL characteristics and their prediction errors are shown in Fig. 6. It is interesting to note that, although we use a "hybrid model" (as $0 < \alpha = 0.75 < 1$) the 15 test points chosen by the QR-decomposition are all points on the DNL characteristic.

5 CONCLUSIONS

We have shown how the model-based testing approach that was originally aimed at INL-specification tests [15] can be extended to yield better performance by using both INL and DNL modeling information simultaneously. With the suggested extended servo-loop measurement setup, it becomes feasible to collect INL and DNL data on the production line, adding a degree of freedom (i.e. the choice between INL and DNL) to the test point selection algorithm to optimize production testing.

The main results presented are based on circuit simulations using SPICE to establish the principle of mixing INL and DNL information. An implementation of the servo-loop method is currently under construction and experimental results are expected to be available for presentation at the conference.

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we used earlier is not sufficiently accurate for our purposes.

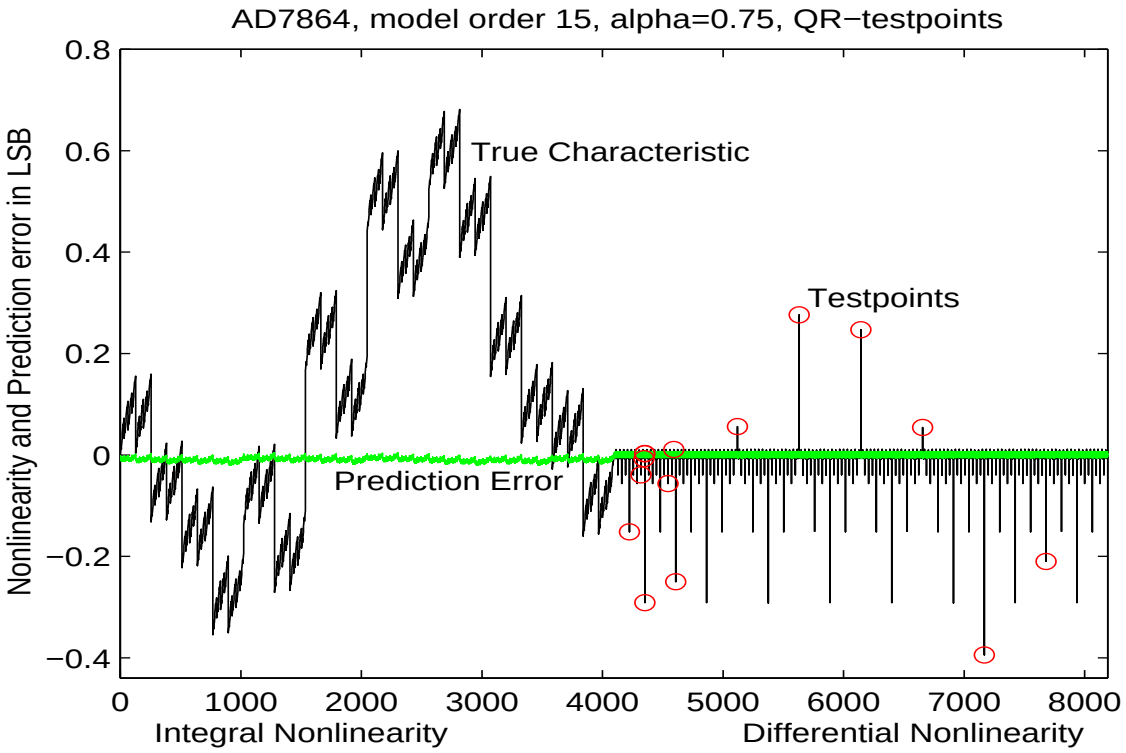

Figure 6: For SPICE-simulated AD7864: INL and DNL (black) with prediction error (gray) predicted by a linear model of order $n = 15$ and parameter $\alpha = 0.75$ using 15 test points (circles).

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