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HARD FAULT DIAGNOSIS IN ELECTRONIC ANALOG CIRCUITS WITH RADIAL BASIS FUNCTION NETWORKS

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Abstract: A Radial Basis Function Network (RBFN) classifier for hard fault location in CMOS analogue circuit is presented. The network is trained by means of a fault dictionary containing the faulty circuit response, which is obtained by simulating the supply current dynamic response.
Keywords: neural networks, fault diagnosis

1 INTRODUCTION

It is well known that fault diagnosis in analog circuits is still an open research field, in spite of test of digital systems for which standardized techniques have been developed.

In analog circuits two types of faults may occur: soft faults, related to deviations of circuit parameters outside their tolerance ranges, these faults do not affect the circuit topology, and hard faults that change the circuit topology. Obviously soft faults are difficult both to diagnose and to locate. In a previous works the authors addressed the problem of single soft faults automated location based on harmonic analysis and a neural classifier. Hard faults can be more easily detected but their location can be difficult and time consuming. This paper presents a technique to locate hard faults in analog CMOS circuits, which proved to be efficient both in terms of time consumption and fault coverage. The proposed technique takes into account hard faults of three types: short circuits, open circuits and Gate Oxide Shorts (GOS) [1].

The proposed methodology is a Simulation Before Test (SBT) technique; hence the more probable faults must be simulated, and characterized by injecting an appropriate input stimulus (or some input stimuli) and by measuring the circuit response at a selected set of test points. The measurement results so obtained are collected in a fault dictionary. The fault location is performed by comparing the circuit under test (CUT) responses to the examples contained in the fault dictionary. It must be underlined that the data contained in the dictionary are a sampling of the set of all the possible faulty circuit responses. Hence the comparison of measured responses with data contained in the dictionary must be performed by a system able to generalize and robust against noise. In this paper we use a neural classifier architecture presented in [2,3] i.e. based on a Radial Basis Function network (RBFN). RBFNs proved to be efficient when used as classifiers since they requires low training time, give an index of the classification efficiency and allow to be up-dated to perform classification of novel faults with a minimum computational effort.

The fault dictionary is formed by considering a single input stimulus and a single test point, in fact we exploit the monitoring of power supply current dynamic response [4]. With this technique a ‘universal node’, the power supply input, is used to reach with the stimulus every component in the circuit and to gather its response.

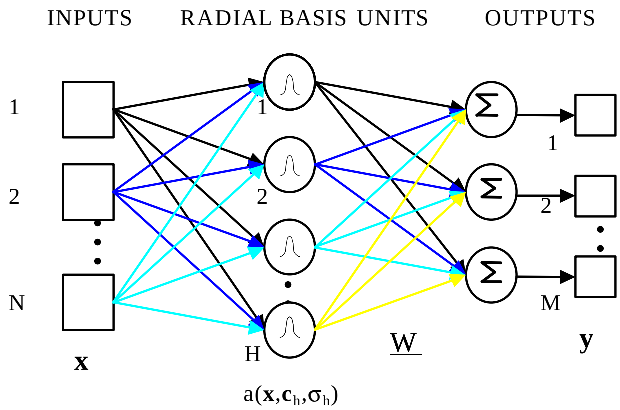
2 RADIAL BASIS FUNCTION NETWORK CLASSIFIERS

RBFNs are layered networks (see figure 1), with the non-linearity in the hidden layer represented by Gaussian functions (radial Basis Functions). Given an input x, the activation a(x) of the hidden units is given by the following equation:

$$a_h(x) = \exp(-\|x - c_h\|^2 / \sigma_h^2) \qquad (1)$$

where c_h represents the position in the input space of the radial basis function and σ_h is the corresponding scaling factor that characterizes the area of the activation region.

The transfer functions of the hidden nodes are non-monotonic in contrast to the monotonic functions of the multi-layer perceptron networks trained with back-propagation algorithms. The connections of the input nodes to the hidden nodes are not weighted and implement a fan-out of the input components to the hidden nodes. As said above, the hidden layer consists of radial units, with Gaussian transfer functions. The finite area of the activation region explains the ability of this network to detect novel cases the network will produce a very low output, since novel cases do not belong to the activation region of any hidden unit. The output layer is made up of M linear summation units, linked to the hidden layer by weighted connections.



(a) (b)

Figure 1(a) RBFN structure. (b) Gaussian Radial Basis Function

Training time is very low since the network can be trained in three sequential steps.

First an unsupervised technique is used, which consists in placing the hidden units layer centers on the centroids of training input clusters. A clustering algorithm is applied to input vectors of the training set to determine cluster centroids. In this research Fuzzy C-Mean clustering algorithm was used to cluster separately data belonging to the different fault classes. In the second step the width of the Gaussian functions is determined and its value depends on the minimum distance among cluster centroids. The output layer weights are trained by a supervised process. A least square regression relates the desired network outputs to the hidden node activations. In fact each training examples is passed through the first layer and the hidden nodes to produce a corresponding hidden node activation vector. The aim is to find the weights that minimize the squared norm of the difference between the desired outputs and the net outputs.

In general the training of the RBF network is an order of magnitude faster than the training of a comparably sized multi-layer perceptron networks trained with back-propagation. On the other hand the RBF are local based network, which usually solve the same problem using a larger number of nodes in the hidden layer than the back-propagation ones.

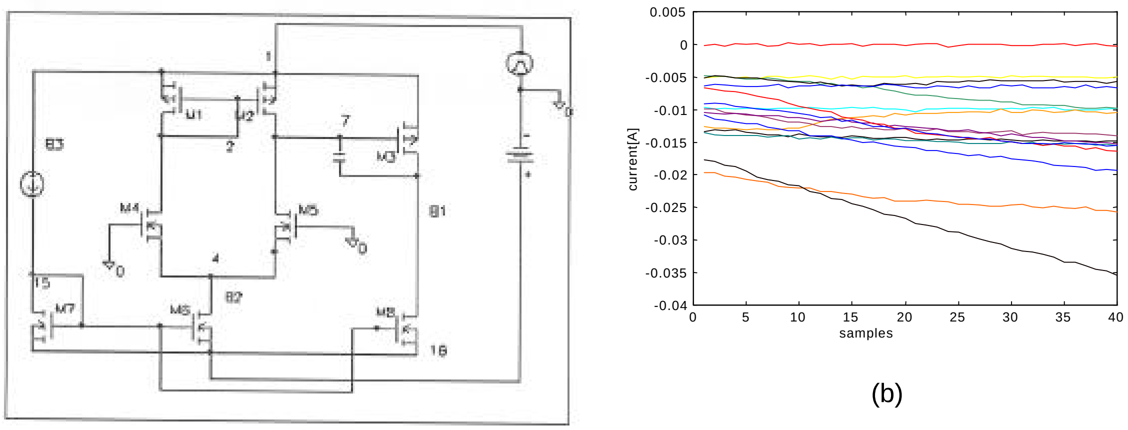
In the paper this network is used as a classifier. The dimension M is equal to the number of fault classes to be detected and each output neuron corresponds to a fault class. The classification criterion is: input belongs to a given fault class if the corresponding output neuron assumes the largest value.

The training set is formed on analogy to that used for the back-propagation classifier. Training input vectors are formed by the circuit supply current signatures given by the circuit when operating in some fault conditions. The target output vectors have a single “1” in the position corresponding to the correct class and “0s” elsewhere.

3 EXPERIMENTAL RESULTS

The proposed technique was applied to some simple operational amplifiers CMOS structures (0.6 μm channel length). For the example shown in figure 2a) a diagnosis system was developed by taking into account the more probable faults. A previous analysis was performed to found ambiguity classes. Each circuit signature in the fault dictionary is obtained by simulating the circuit using PSPICE, when a positive ramp is applied to the positive power supply input, while the negative power supply is kept at the default value. The signal inputs are shorted to ground. For the GOS faults we use the models developed in [1]. Each fault was injected in the circuit by modifying appropriately its topology, and the related circuit signature is obtained. To account for possible spread of MOS parameters, we use Monte Carlo analysis, and we let vary some MOS parameters (VTO, KP, TOX, XJ, RHS etc..) with a Gaussian distribution. For each parameter the mean is assumed equal to the nominal value while the standard deviation is derived from data concerning different runs of the same foundry process. Accounting for parameter deviations, a family of supply current responses was obtained for each fault class.

In figure (2b) a single signature for a subset of possible faults is shown. The measurement error is accounted for by superimposing to the circuit signature a white Gaussian noise with zero mean. Some results obtained by the presented fault diagnosis system for the circuit in figure (2a) are shown in figure (3), where a Signal to Noise Ratio (SNR) of 40dB was considered. In the figure the classification error is shown as a function of the number of hidden nodes.



(a)

Figure 2 (a) CMOS Circuit Under Test. (b) Examples of the circuit signatures

It is well known, in fact, that for RBF networks the size of the hidden layer is a key factor. In this paper the hidden node number is selected by evaluating the performance of the RBF network: i.e. by observing the rate of classification error, during training and during normal net operation, and by selecting the hidden node number which corresponds to the minimum classification error. It must be noted that too low a hidden node number gives a net that can not be trained adequately. On the other hand, a net with too many hidden neurons (near to the condition a hidden node for each training example) can give very low rates of error during training but may be unable to generalize and give a high rate of errors during normal operations.

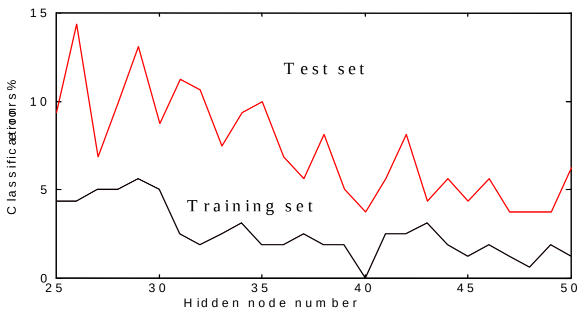


Figure 3 classification errors for circuit in figure (2) as a function of RBFN hidden nodes'nuber.

The net was trained with 10 noisy examples of 16 fault classes signatures made up of 20 time samples. The considered fault classes for this circuit are listed in table 1. A test set of 400 signature was used. It can be seen that the error falls below 5% for a net with a reasonable complexity (40 hidden nodes). The net performs well even in presence of noise; it can be seen, in fact, that with SNR higher than 30 dB, the net gives the same results as in the noise free case.

Table 1 Fault classes for the circuit in figure 2a).

BC 0	Operating circuit (fault free)	**BC 9**	Short circuit between nodes 4 and 15
BC 1	short circuit between nodes 1 and 2	**BC 10**	Short circuit between nodes 1 and 15
BC 2	short circuit between nodes 1 and 7	**BC 11**	Short circuit between nodes 2 and 15
BC 3	short circuit between nodes 2 and 4	**BC 12**	GOS between gate and drain di M8
BC 5	Branch 1 open	**BC 13**	GOS between gate and source of M5
BC 6	Branch 3 open	**BC 14**	GOS between gate and drain of M5
BC 7	Branch 2 open	**BC 15**	GOS between gate and drain ofM4
BC 8	short circuit between nodes 4 and 16	**BC 16**	GOS between gate and drain of M6; GOS between gate and drain of M8

The same methodology was applied also to the circuit in figure (4), where 9 fault classes were taken into account (short circuits, open circuits and more probable GOSs). For this circuit, tested with a set of 180 vectors characterized by a SNR of 40 dB, similar results were obtained: the classification error was 4% with 18 nodes in the hidden layer.

4 CONCLUSIONS

An automated diagnosis technique to locate hard fault in analog CMOS circuits was presented. A single measurement performed on the supply input was used to obtain a time domain fault signature. The effect of both component parameter spread and measurement noise was taken into account. The proposed technique is based on the application of a neural classifier with the advantage of a reduced training time. Moreover the classifier architecture is flexible and allows the addition of new fault classes, with a low additional computational burden. In fact new fault classes require to train again only the output layer and to perform clustering on the newly added example data set. The proposed technique has good performance, and the classification errors for the analyzed circuits remains near 5%.

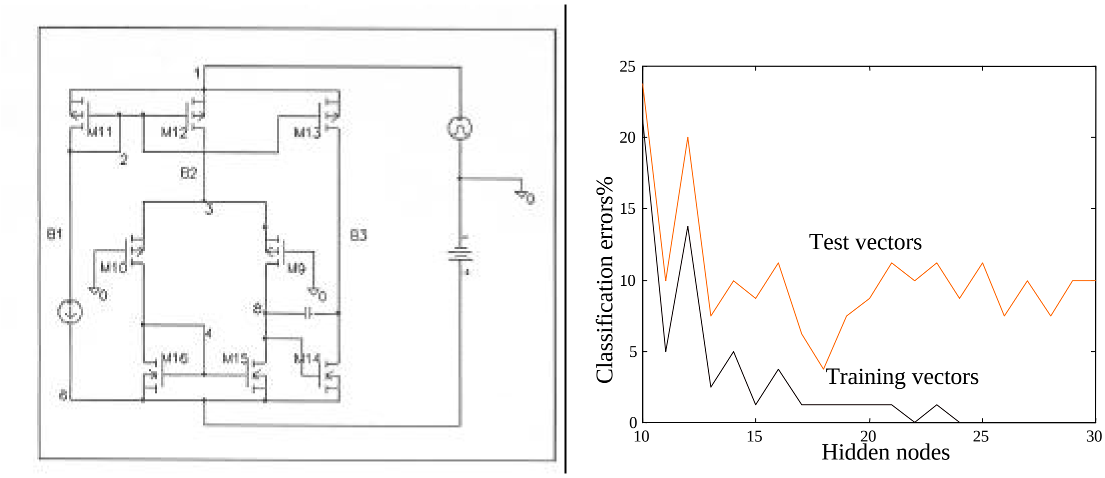


Figure 4 (a)Circuit under test;(b) classification errors as a function of hidden nodes' number.

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