

# PIECEWISE LINEAR CIRCUIT DIAGNOSIS BASED ON COMPONENT CONNECTION MODEL

*A. Robotycki, R. Zielonko*

Chair of Electronic Measurement

Faculty of Electronics, Telecommunications and Informatics

Technical University of Gdansk, 80-952 Gdansk, Poland

*Abstract: The paper presents the method of fault location of the piecewise linear type analog circuits based on the verification approach and the component connection model. For verification of the fault hypothesis the residual square sum criterion is applied. In the first part of the paper the diagnostic equations describing the model and the algorithm of the method are presented. Theoretical considerations have been illustrated on the example of single and double fault diagnosis of the three-stage transistor amplifier.*

*Keywords: diagnosis, piecewise linear circuits, component connection model.*

## 1 INTRODUCTION

Development of nonlinear analog and mixed-signal circuits creates the necessity of elaboration new, efficient methods of their fault location (and alternatively identification). Unlike to the fault diagnosis of linear circuits, the diagnosis of nonlinear ones is much more complicated. It follows from existence of multiple solutions of nonlinear circuit equations and bias shifting of nonlinear components. It may cause fault-free circuit will appear as faulty. Additional difficulty is limited accessibility to internal nodes of circuit under test (CUT). Some above difficulties can be omitted in case of piecewise linear (PWL) circuits [1].

The paper presents the method for fault diagnosis of PWL circuits with parametric faults, without a priori information about the number of faults. A domain of the diagnostic equation, describing the circuit under test, is partitioned into regions, inside whose the equation is linear [2]. Because all nonlinearities are located in the region boundaries, being the hyperplanes, the linear diagnostic method can be used in each region separately. It gives the possibility to use the verification technique, which has been developed for diagnosis of linear circuits.

The method is based on the component connection model (CCM) proposed by Saeks [3] and PWL models of nonlinear elements [4]. By using the CCM the diagnostic equation can be easily formulated in comparison to other approaches (hybrid and Tableau models [5,6]). For verification of fault hypotheses the residual square sum criterion is applied. The verification process is performed for all hypotheses in all regions for adequate diagnostic equations.

In Sections 2-4 of the paper, the PWL parametric description of nonlinear characteristic, diagnostic equation, a fault location algorithm and an algorithm for reduction of hypotheses are described. In Section 5, the method is illustrated on the example of single and double fault diagnosis of the three-stage transistor amplifier. Finally, conclusions are included in Section 6.

## 2 CIRCUIT DIAGNOSIS AND PWL MODEL

One of a few diagnosis methods for linear circuits with limited accessibility is the verification method. This method is based on an assumption of a hypothesis that some  $f$  branches in a circuit with  $b$  branches ( $f < b$ ) are faulty. For this hypothesis the reduced diagnostic equation is formulated and verification is performed. In a tolerance less case, the hypothesis verification consists in testing the linear dependence between discrepancy vector of nominal and measured signal responses and the diagnostic matrix of the reduced diagnostic equation. If the linear dependency has occurred, the variables of excitation vector show faulty branches of the CUT. If the hypothesis is not true, other set of faulty branches is assumed and the verification process is repeated [5].

In this paper we apply the verification approach to fault diagnosis of PWL circuits. Due to lack of information about the region of faulty circuit, the diagnostic equation has to be created for each linear region separately.

The method is based on the PWL models of nonlinear components of the CUT shown in Figure 1. In the Figure 1a, the conventional current-voltage PWL characteristic is presented. Each segment  $s_1, \dots, s_4$  can be described by a segment slope  $G_i$  and an intersection point  $I_i$ . These coefficients are parameters of the PWL model of a nonlinear component. Because  $G_i$  and  $I_i$  can not be seen by direct

reading from the PWL characteristic we propose an alternative form of PWL representation, shown in Figure 1b. Such representation is more convenient for use in PWL diagnosis, because segment parameters  $G_i, l_i$  are directly used in computing, have clear physical interpretation and are easy to reading from a graph or a table.

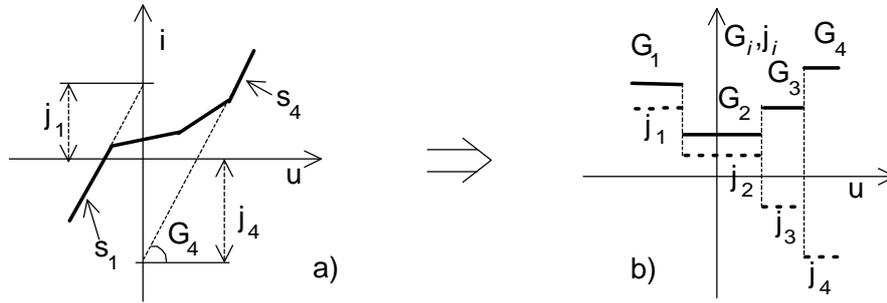


Figure 1. a) Conventional PWL characteristic of a component.  
b)  $G_i, l_i$  parametric characteristic description.

### 3 COMPONENT CONNECTION DIAGNOSTIC EQUATION

In previous papers we reported diagnosis methods based on the Tableau approach [6] and the multiport hybrid model [5]. In this work we propose the method, which is based on the diagnostic

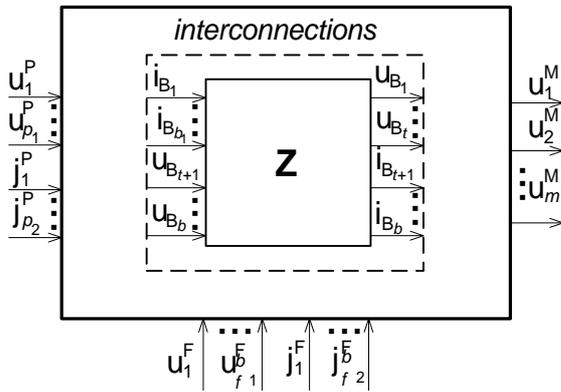


Figure 2. Component connection model.

equation using component connection model [3], shown in Figure 2. The model consists of a box of components  $Z$  and a space of connections between inputs  $\mathbf{x}^P, \mathbf{x}^F, \mathbf{b}$  and outputs  $\mathbf{a}, \mathbf{y}^M$ , where  $\mathbf{x}^P = [u_1^P, \dots, u_{p_1}^P, j_1^P, \dots, j_{p_2}^P]^T$  is the input excitation vector at external nodes ( $p_1, p_2$  – number of voltage and current excitation respectively),  $\mathbf{x}^F = [u_1^F, \dots, u_{b_{f_1}}^F, j_1^F, \dots, j_{b_{f_2}}^F]^T$  is the vector of voltage and current sources modelling perturbations of faulty elements,  $b_{f_1}, b_{f_2}$  are numbers of voltage and current fault sources correspondingly,  $\mathbf{b} = [u_{B_1}, \dots, u_{B_t}, i_{B_{t+1}}, \dots, i_{B_b}]^T$ ,

$\mathbf{a} = [i_{B_1}, \dots, i_{B_t}, u_{B_{t+1}}, \dots, u_{B_b}]^T$  represent the vectors of

the output and the input variables of the components respectively ( $t$  is number of tree branches in graph of circuit model,  $b$  denotes number of all component branches in the graph) and  $\mathbf{y}^M = [u_1^M, \dots, u_m^M]^T$  is the output measurement vector of the system responses. We assume only node voltage measurements.

In the single region the PWL model of the CUT with  $m$  measurement nodes is described by equations:

$$\begin{bmatrix} \mathbf{a} \\ \mathbf{y}^M \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{11} & \mathbf{L}_{12} \\ \mathbf{L}_{21} & \mathbf{L}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{b} \\ \mathbf{x} \end{bmatrix}, \quad \mathbf{x} = \begin{bmatrix} \mathbf{x}^P \\ \mathbf{x}^F \end{bmatrix}, \quad (1)$$

$$\mathbf{b} = \mathbf{Z}\mathbf{a}, \quad (2)$$

$$\mathbf{y}^M = \mathbf{S}\mathbf{x}, \quad \mathbf{S} = \begin{bmatrix} \mathbf{S}^P & \mathbf{S}^F \end{bmatrix}. \quad (3)$$

$\mathbf{L}_{11}, \mathbf{L}_{12}, \mathbf{L}_{21}$  and  $\mathbf{L}_{22}$  are interconnection matrices (usually sparse) describing the circuit topology. These matrices are formulated on the basis of the tree/cotree of circuit graph. The matrix  $\mathbf{S}$  is the nominal system transfer matrix,  $\mathbf{S}^P$  and  $\mathbf{S}^F$  are submatrices, whose columns are associated with input measurements and with adequate potentially faulty elements, respectively. On the basis of (1), (2) and (3) we obtain the matrix  $\mathbf{S}$  of the overall circuit

$$\mathbf{S} = \mathbf{L}_{21}(\mathbf{1} - \mathbf{Z}\mathbf{L}_{11})^{-1}\mathbf{Z}\mathbf{L}_{12} + \mathbf{L}_{22}. \quad (4)$$

For the CUT with  $b$  branches and  $n_e$  nodes ( $n_e$  – number of nodes excluding reference node) we can formulate the necessary condition of  $\mathbf{S}$  matrix existence as  $b=2n_e$ . If this condition is not satisfied, we can not obtain the matrix  $\mathbf{S}$  and the diagnosis can not be performed.

Because faulty element deviations are outside the CCM, the matrix  $\mathbf{S}$  includes only nominal values of the component parameters. For the fault-free circuit  $\mathbf{x}^F=0$  and the component connection equation takes the form

$$\mathbf{y}_0^M = \begin{bmatrix} \mathbf{S}^P & \mathbf{S}^F \\ \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{x}^P \\ \mathbf{0} \end{bmatrix}, \quad (5)$$

where  $\mathbf{y}_0^M$  is the output measurement vector of fault-free circuit. Using the discrepancy output vector of the real and the fault-free circuit

$$\Delta \mathbf{y}^M = \mathbf{y}^M - \mathbf{y}_0^M, \quad (6)$$

we get from (3) and (5) the component connection diagnostic equation (CCDE)

$$\Delta \mathbf{y}^M = \mathbf{S}^F \mathbf{x}^F. \quad (7)$$

On the basis of Eq. (7) we create reduced component connection diagnostic equations (RCCDE), whose are associated with adequate fault hypotheses. Similarly as in verification approach for linear analog circuits, first we assume single fault hypotheses, next double fault ones until  $f$  fault hypotheses ( $f \leq m-2$ ). If only single fault happens, the verification process is finished, else we have to verify hypotheses for more faults. Assuming  $q$  faults ( $q \leq f$ ) for  $k$  hypothesis we formulate the set of potentially faulty elements as  $c_{qk}$ . For this set  $c_{qk}$  we obtain the RCCDE as

$$\Delta \mathbf{y}^M = \mathbf{S}^{Fc_{qk}} \mathbf{x}^{Fc_{qk}}. \quad (8)$$

The submatrix  $\mathbf{S}^{Fc_{qk}}$  is obtained from the matrix  $\mathbf{S}^F$  by saving columns connected with hypothetical faulty elements and cutting rest columns, as shown in Figure 3.

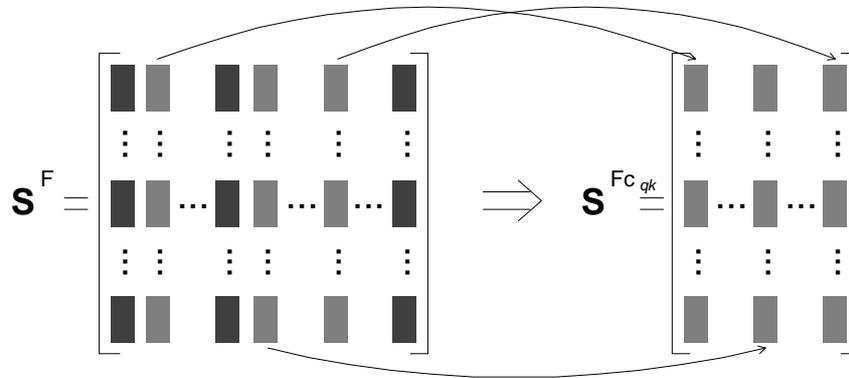


Figure 3. Formulation  $\mathbf{S}^{Fc_{qk}}$  from  $\mathbf{S}^F$ .

On the basis of the RCCDE (8) we can verify assumed hypothesis. The influence of element tolerances does not allow using the linear dependency criterion mentioned for hypothesis verification and estimation criterions must be applied. We found as the most useful the residual number criterion, which is based on the least square sum described as

$$\mathbf{r} = (\Delta \mathbf{y}^M)^T \mathbf{S}_r \Delta \mathbf{y}^M, \quad \mathbf{S}_r = \left[ \mathbf{1} - \mathbf{S}^{Fc_{qk}} (\mathbf{S}^{Fc_{qk}})^+ \right]. \quad (9)$$

For this criterion a residual threshold  $\Delta r$  is formulated

$$\Delta r = \begin{cases} 1, & r_{dis} \leq r_{nom} \\ 0, & r_{dis} > r_{nom} \end{cases}, \quad (10)$$

where  $r_{dis}$ ,  $r_{nom}$  denote the residual numbers for potentially fault and fault-free circuit respectively. The residual threshold  $\Delta r$  sets the boundary value for hypothesis verification. For  $\Delta r=1$  the hypothesis is true and for  $\Delta r=0$  is false.

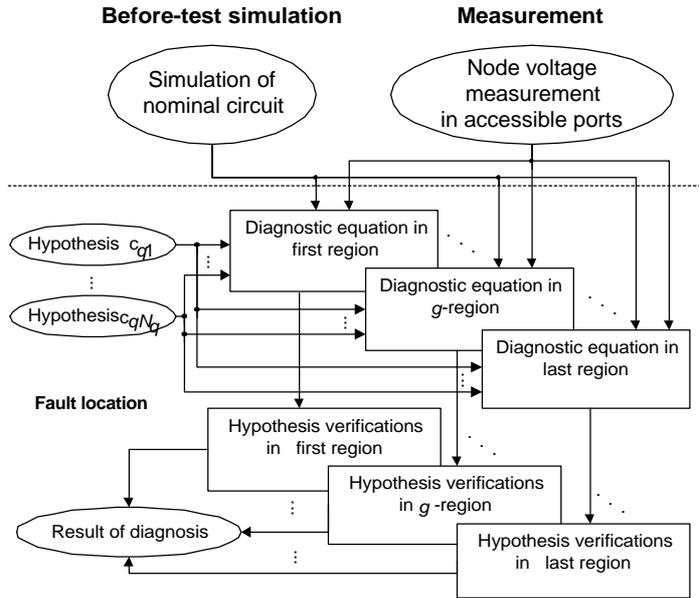


Figure 4. Fault location algorithm.

The most probably set of faulty components associated with verified hypothesis can be found for minimum  $r_{dis}$  and for  $\Delta r=1$  in the investigated region.

The fault location algorithm, shown in Figure 3, can be recapitulated followings:

1. For each region formulate the component connection diagnostic equation (7).
2. In each region define the sets  $c_{qk}$  for fault hypotheses. For each hypothesis formulate the reduced hybrid equations and calculate matrices  $S_r$ .
3. Compute  $r_{dis}$  and  $r_{nom}$  for each hypothesis and each region. If  $\Delta r=1$  then the associated hypothesis is taken under consideration in further analysis.
4. Find in all regions the minimum value  $r_{dis}$ , for which  $\Delta r=1$ . Hypothesis connected with this value indicates the most probably set of faulty components.

#### 4 ALGORITHM FOR REDUCTION OF HYPOTHESES

For PWL circuits, the number of regions as well as the number of hypotheses increases significantly with a growth of PWL elements. The verification time is then longer. Therefore, it is reasonable to look for effective methods for reduction of hypotheses, in order to determine the range of region changes of CUT for changes several component parameters. Some approaches can be used for this purpose, for example before-test analysis, a priori information, partitioning technique etc.

In this paper we propose the method based on the before-test analysis [5]. For deviations of individual components in assumed bounds, minimal  $IS_{min}$  and maximal  $IS_{max}$  segment indexes of PWL components are calculated. For these indexes, number of segments for assumed component changes is calculated

$$NS=IS_{max}-IS_{min}+1. \tag{11}$$

In [7] B. Kaminska and M. Slamani divided deviations of parametric faults as soft and large-deviations. Soft faults mean small changes of component parameters, while in the case of large deviations, the faulty component can change to 50% from its nominal value. We propose one more fault class with very large deviations, where the components vary to 90%.

The number of reduced regions  $NH$  [5], in whose hypotheses are verified, is

$$NH = \sum_{k=1}^{N_q} \left( \prod_{j=1}^n NS_{j,c_{qk}} \right), \tag{12}$$

where  $NS_{j,c_{qk}}$  is the range of segment changes for selected PWL component with the assumed very large deviations of the components from  $c_{qk}$  set,  $N_q$  – number of hypotheses for  $q$  faults and  $n$  is the number of PWL components.

#### 5 EXAMPLE

The method has been verified on the example of the three-stage transistor amplifier shown in Figure 5. The nodes 1,2,5,9 and 10 of the circuit under test are accessible for voltage measurement ( $m=5$ ). PWL model of the circuit has  $n=6$  PWL elements (there are 6 diodes from 3 Ebers-Moll models of transistors). The characteristic of each PWL element consist of 7 segments ( $L_r=7$ ). So, the total number of regions is  $K = (L_r)^n = 117649$ .

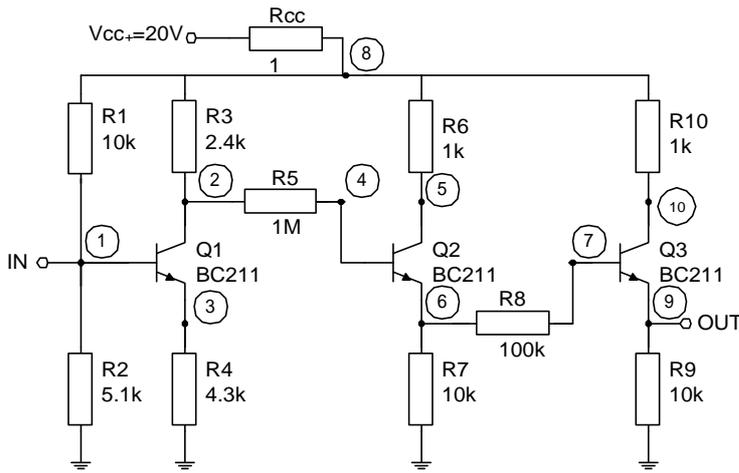


Figure 5. The three-stage transistor amplifier.

The cotree of the circuit graph contains current dependent sources (from transistor Ebers-Moll model) and in the tree are controlling currents for these sources.

In this example the possibility of single and double faults for 10 resistors and all transistor parameters ( $b_F = b_{F1} + b_{F2} = 22$ ) has been analysed. To reduce the number of possible hypotheses the reduction algorithm, mentioned above, is used. In Table 1 results for some selected components are presented. The reduced number of regions is  $NH=411$ . So, after the reduction, the verification of the hypotheses has to be performed only in 0.3% all possible regions,

time of diagnosis significantly decreases.

Table 1. The range of segment changes for  $U_{BE}$ ,  $U_{BC}$  of transistors with 90% component deviations.

Component	Q1		Q2		Q3	
	$NS_{UBE}$	$NS_{UBC}$	$NS_{UBE}$	$NS_{UBC}$	$NS_{UBE}$	$NS_{UBC}$
R1=10k $\Omega$	6	7	1	1	1	1
R3=2.4k $\Omega$	1	7	1	1	1	1
R4=4.3k $\Omega$	1	7	6	1	6	1
R6=1k $\Omega$	1	1	1	7	6	1
R8=100k $\Omega$	1	1	1	1	1	1
$\alpha_{F1}=0.992$	1	1	1	1	1	1
$\alpha_{F3}=0.9895$	1	1	1	1	1	1

Two examples have been considered: one single fault and one double fault. In both cases, the hypotheses verification has been performed for  $NH=411$  regions.

For the single fault diagnosis, the diagnosis time on the computer with processor Pentium Celeron 433MHz equals about 2s. Results of residual numbers  $r_{dis}$  for 5 selected fault hypotheses in 42 regions are shown in Figure 6a.

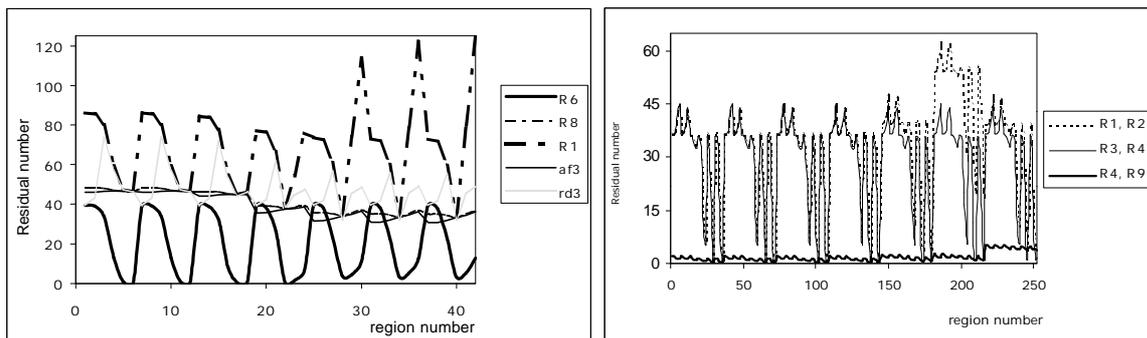


Figure 6. The residual numbers  $r_{dis}$  of some components in selected regions for deviations of a) the single fault diagnosis b) the double fault diagnosis.

The bold, continuous line describes the fault hypothesis of the resistor R6. The rest of lines describe the hypotheses associated with faults: of the resistors R8, R1,  $a_f$  of the transistor Q3 and the resistance  $rd3$  of base-emitter junction of the transistor Q2. Values of  $r_{dis}$  for R6 are minimal in all examined regions. Because the residual number denotes the least square distance from the real object to its model,  $r_{dis}$  value nearly zero is associated with the model of the object, which is nearly the real object. Therefore, the minimal  $r_{dis}$  has been analysed in 42 regions for R6. This residual number has 7 minimums, picked in Table 2. In the table, the segment indexes of PWL components are

presented in the order:  $rd1(ld1), \dots, rd6(ld6)$ , where indexes 1,3,5 are connected with base-emitter junctions and indexes 2,4,6 with base-collector junctions of transistors Q1,2,3 respectively.

Table 2. Minimum values of  $r_{dis}$  for R6 in 42 selected regions.

Region	6	12	17	22	28	34	40
$r_{dis}$ value	0.02	0.02	0.25	0.18	3.66	3.2	3.11
Segment Indexes	7,1,7,1,7,1	7,1,7,2,7,1	7,1,7,3,6,1	7,1,7,4,5,1	7,1,7,5,5,1	7,1,7,6,5,1	7,1,7,7,5,1

It is seen from the table 2 that the minimum  $r_{dis}$  are in regions 6 and 12, for two segments of the resistance  $rd4$ . The rest of minimums is at least one rank larger, so the resistor R6 is found as the most probably faulty element. The faulty circuit is in region described by the segments: 7,1,1-2,7,1. This ambiguity, for both 1st and 2nd segments, is caused by similar  $rd4$  values and by  $ld4$  equal zero. The result of diagnosis is agreed with the real fault of the CUT, where the resistance R6 was changed from  $1k\Omega$  to  $10k\Omega$ .

In the case of the double fault diagnosis, results for 3 selected hypotheses in 252 selected regions are shown in Figure 6b. The bold, continuous line describes the fault hypothesis of two resistors: R4, R9. For this hypothesis, values of  $r_{dis}$  are minimal in all examined regions. Therefore, resistors R4, R9 denote the most probably set of faults. The CUT was faulty by deviating two resistances R4 and R9 from  $R4=4.3k\Omega$ ,  $R9=10k\Omega$  to  $R4=7k\Omega$ ,  $R9=3k\Omega$ . The diagnosis time equals 30s.

The diagnosis time increases significantly with the growth of faults. Due to the increase of hypotheses, the number of hypotheses for  $q$  faults is described as  $C_{bF}^q$ .

## 6 SUMMARY

In the paper we presented the fault diagnosis method of PWL analog circuits, which essential features are: the extension of the verification approach on nonlinear PWL circuits and using component connection model as well as residual number criterion for hypotheses verification.

The advantage of the model is simplicity of diagnostic equation formulation in comparison to the hybrid multiport model and the Tableau model. Computing effort of the method is greater, but calculations are performed at once in before test stage. Other advantage of the method is possibility of circuit diagnosis not only on the level of to faulty element but also faulty block, which is important in test bus applications. By using the parametric description of the PWL models as well as by applying the proposed hypotheses reduction, it is possible to obtain the reasonable diagnosis time (2s for single fault diagnosis of the circuit with 3 transistors and 10 resistors).

In present form the method can be used in libraries of conventional testing systems of PCB and in systems with IEEE P1149.4 test bus. There are possibilities of its improvements by taking into account tolerances and choosing of measurement nodes on the basis of sensitivity criterions.

## REFERENCES

- [1] R. Liu, Testing and diagnosis of analog circuits and systems, *Van Nostrand Reinhold*, New York, 1991.
- [2] M. Tadeusiewicz, Metody komputerowej analizy sta³opr¹dowej nieliniowych uk³adów elektronicznych, *WNT*, Warszawa 1991.
- [3] R. Saeks, S. R. Liberty, Rational Fault Analysis, *Marcel Dekker Inc.*, New York and Basel, 1977, p. 124-133.
- [4] W. Toczek, R. Zielonko, A. Adamczyk, A method for fault diagnosis of nonlinear electronic circuits, *Measurement*, vol. 24, 1998, pp. 79-86.
- [5] A. Robotycki, R. Zielonko, Fault diagnosis method for analog PWL circuits based on hybrid approach, *Metrologia i Systemy Pomiarowe*, nr 1, 2000.
- [6] A. Robotycki, W. Roczek, Metodyka diagnostyki uszkodzeñ uk³adów i systemów nieliniowych opisywanych charakterystykami odcinkowo-liniowymi, *XXIX Miedzynarodowa Konferencja Metrologów*, Naë czów, 10-12 wrzœnia 1997, Tom 2, pp. 477-484.
- [7] M. Slamani, B. Kaminska, Multifrequency Analysis of faults in Analog Circuits, *IEEE Design & Test of Computers*, Summer 1995, p. 70-80.

**AUTHORS:** MSc Ing. Artur ROBOTYCKI, Prof. Dr Ing. Romuald Zielonko, Chair of Electronic Measurement, Faculty of Electronics, Telecommunications and Informatics, TU of Gdansk, Narutowicza 11/12, 80-952 Gdansk, Poland, Phone Int +0048 583471457, +0048 583472255, Fax Int +0048 583472255, E-mail: arobot@eti.pg.gda.pl, zielonko@pg.gda.pl.