XVIII IMEKO WORLD CONGRESS
Metrology for a Sustainable Development
September, 17 – 22, 2006, Rio de Janeiro, Brazil

Developing Model-Based Design Evaluation for Algorithmic A/D Converters

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Abstract: In this paper we propose a novel Design Evaluation concept suitable for Nyquist-rate A/D converters employing the recently introduced technique of LEMMA (Linear Error Mechanism Modeling Algorithm). The core of our methodology is a root-cause identification of the error sources present in the ADC structure, evaluating the performance degradation by static non-linearity in a series of consecutive steps. Our solution benefits a wide scale of design optimization and device calibration possibilities, as it is demonstrated on a design example of Switched-Current (SI) algorithmic ADC. The results introduced in this paper are proven by full-transistor level and behavioral ADC simulation, back-annotating the parameters of its basic circuit element (SI memory cell) from the measurement of available silicon samples.

Keywords: Design Evaluation, analog testing, error mechanism, linear modeling, Switched-Current, Nyquist-rate A/D converter.

1. INTRODUCTION

The process of Design Evaluation requires one to verify whether the implementation of a design conforms to its specifications. In an A/D converter case, the Design Evaluation task becomes especially difficult; an ADC builds a typical example of mixed-mode system comprising a number of analog parameters which need to be verified for a set of digital states (output codes). Specifically, the Design Evaluation process is often focused to significant ADC performance metrics, such as *INL* and *DNL* (*integral* and *differential non-linearity*). Currently used Design Evaluation approaches are often based on ad-hoc methods using the designer's intuition and previous experience. The verification process carried out in this "trial and error" way usually takes an exhaustive time, giving no possibility of subsequent *design optimization* and *calibration* (labeled also as *design streamlining*).

1.1. LEMMA-based Design Evaluation

Recently, an advanced LEMMA-based approach for Design Evaluation and modeling of data converters has been developed. The LEMMA method [1], [2] is capable to overcome the above-mentioned problems, exploiting the relationship between the error sources present in the IC design and the extracted (simulated or measured) ADC non-linearity. The LEMMA uses a linear model concept based on the fact that the system accuracy of the analog portion of a Nyquist-rate ADC is usually by orders higher compared to the equivalent signal change of 1LSB. Under this condition, LEMMA is capable to predict the ADC performance for the full set of output codes, effectively reducing the time and cost requirements during the whole process of IC design and manufacturing. Note that the LEMMA method is particularly suited for problems where the number of significant inputs is much greater than the number of error producing mechanisms [1]. This is especially the case of data converters where the number of error sources contributing to the device response is much smaller than the number of analog parameters and digital states of the system under verification. Despite its excellent abilities, the LEMMA is described quite rarely in the recent applications [3], [4].

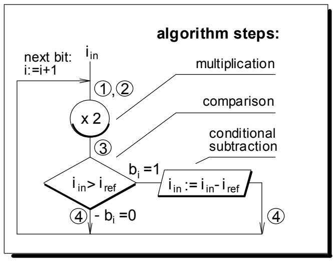

Fig. 1. ADC conversion algorithm.

1.2. A Novel Concept Proposed in This Work

In this contribution we propose a novel step-by-step Design Evaluation concept suitable for Nyquist-rate A/D converters. In further text, the main asset of our work will be presented, giving the main stress on the following topics:

- developing a novel implementation of the LEMMA-aided Design Evaluation suitable for *algorithmic class of data converters,*
- formulation of *generic streamlining guidelines* and their confirmation on an ADC design optimization and calibration example,

- demonstration of *significant time reduction* both in simulation and test by maintaining a very good accuracy, as a result of the advanced modeling techniques used.

To extend the application field of LEMMA, we demonstrate the benefit of our solution on an example of algorithmic ADC structure realized by the Switched-Current (SI) design technique. Here, the basic SI memory cell acts as a current-mode sample-and-hold circuit being fully compatible with modern CMOS VLSI processes. The algorithmic ADC structure employing SI memory cells is very simple and straightforward, as a result of its cyclic operation and hardware re-use. Such design transparency creates an ideal opportunity to streamline its circuit solution applying the LEMMA-based approach presented in this article.

In Sec. 2, we describe the architecture and design implementation of the Switched-Current ADC considered for the Design Evaluation. Sec. 3 proposes the novel Design Evaluation procedure divided into consecutive steps. The results of our approach are continuously documented in Sec. 3.1 to 3.4 by a generic guidelines starting at extraction of ADC performance and concluding with model-based ADC design streamlining. Sec. 4 draws the work conclusions.

2. CONSIDERED ADC STRUCTURE

2.1. Architecture and Conversion Algorithm

The considered ADC architecture proceeds bit-by-bit serial conversion, for which the single-quadrant non-restoring algorithm was chosen. The basic conversion scheme (Fig. 1) comprises three algorithmic operations referred to as *multiplication*, *comparison* and *conditional subtraction*. First, the input current i_{in} is multiplied by two and then compared with the current reference value of i_{ref}. If the input value is greater than the reference, the converted bit is one while subtracting the reference value from the input signal. Otherwise, the converted bit is zero and no subtraction is performed. Then the algorithm proceeds with the next less significant bit (the loop is repeated until the least significant bit LSB is converted).

2.2. Design Implementation and Model

The ADC is implemented as an eight-bit Switched-Current algorithmic design containing more than 300 transistors in the analog part. The ADC circuit solution employs several techniques to improve the target performance [5]. For example, it features a high precision structure of SI memory cell labeled as “S3I-GGA-casc” [6] which was prototyped on silicon and successfully measured. A behavioral model of the proposed ADC is depicted in Fig. 2a. It comprises an *input stage, SI memory cells* PN1 to N4 and a *comparator* with MX&LATCH circuit. Input current signal i_{in} is converted into a serial binary word, available at the DATA output. The ADC conversion process follows the timing signals as shown in Fig. 2b, dividing the whole operation into phases ① to ④. Here, a direct correspondence is apparent from the identification with the algorithm steps displayed in Fig. 1 – see the description in [5] for more details. The whole ADC model is built as “circuit-similar”, respecting the non-ideal properties and functionality of the building blocks. The first error included in the model is the *charge injection (CHI)* being related to the channel charge of the memorization switch in a SI memory cell. Secondly, *input-over-output resistance ratio (RIO)* is statically defined on the SI memory cell ports. As the next, LAMBDAREL error denotes the signal-dependent output conductance of the memory cell, caused by the channel-length modulation of the memorization transistor. The ADC input stage gives rise to the fourth error labeled as *GREF* which represents the *internal conductance* of the reference current source. Finally, the comparator block is described by its first-order static model characterized by the *voltage offset (VOS)* parameter.

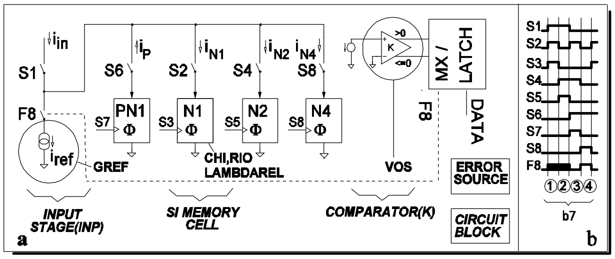

Fig. 2. ADC behavioral model: a) structure, b) timing forces (MSB conversion example).

3. PROPOSED DESIGN EVALUATION PROCEDURE

3.1. Extraction of ADC Design Performance

The first step is to extract the ADC performance characterized by the INL and DNL, from the existing transistor-level design. Compared to conventional approaches, the set of code testpoints required by LEMMA is significantly reduced. From the whole set of 255 points corresponding to the eight-bit ADC resolution, only those at *major transitions* of the algorithmic architecture need to be selected [2]. In this work we apply the *servo-loop* method [7] to extract the *static* ADC performance by highly-accurate analog simulation in ELDO 6.2. For this purpose a versatile program unit in Verilog-A was created, achieving significant improvements in the target algorithm resolution

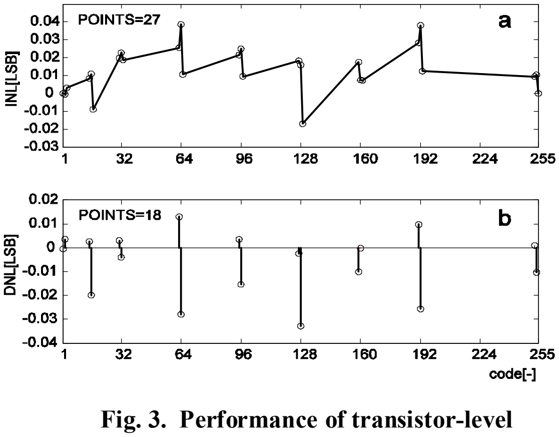

Fig. 3. Performance of transistor-level ADC design: a) INL, b)DNL.

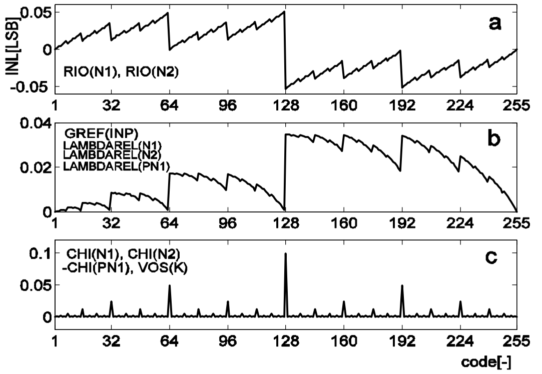

Fig. 4. Ambiguity groups of error sources in the ADC model: a) GAIN1, b) GAIN2, c) OFFSET1.

and convergence. Simulated INL and DNL plots are in Fig. 3, showing that the maximum values are lower than 0.04 LSB. Note that this high performance level obtained implies to the robust ADC design described in [5]. The CPU simulation time per one code was approx. 30 hours, implying that the total simulation effort required for the subset of 27 codes was more than 33 days. To reduce this exhaustive time, the simulation was performed on several PCs in parallel.

3.2. Identification of ADC Parameters

The second step in the ADC Design Evaluation is to identify the parameters which affect the target performance. The ADC performance is represented by non-linearities; in our case we choose the INL characteristic extracted in the previous step as the most significant metric. Subsequently, we start to implement the LEMMA procedure which is capable to systematically isolate individual performance contributors - *error sources*. In the sense of the ADC architecture (Sec. 2.1), an error source means a non-ideality acting at a certain phase of the ADC conversion process. It can have a multiplicative or additive nature depending on which conversion phase it is attached to; a *GAIN* error source represents a multiplicative process (such as the multiplication carried out in phases ① to ③, see Fig. 1) whereas an *OFFSET* error source can be related to every additive operation (for example comparison being performed within phases ③ and ④ by a simple current subtraction). As it concerns the ADC design implementation (Sec. 2.2), every circuit block with its non-ideality (e.g. the comparator with its voltage offset) can be represented by an equivalent error source having the same influence on the INL characteristic (such as VOS in our case). The corresponding assignment process is denoted as *identification*; for simplicity, the same annotation applies for a circuit non-ideality and an appropriate error source. Performing the identification procedure, some error sources can exhibit a *linear dependence* if one pattern is a multiple of the other. Such error sources can not be distinguished by any external analysis of the INL characteristic and can be thus joined into an *ambiguity group* [8]. The identification procedure ends up with an attachment of the known error sources to the ADC model (Fig. 2). The procedure stated above takes the following advantages over a conventional approach (Sec. 1).

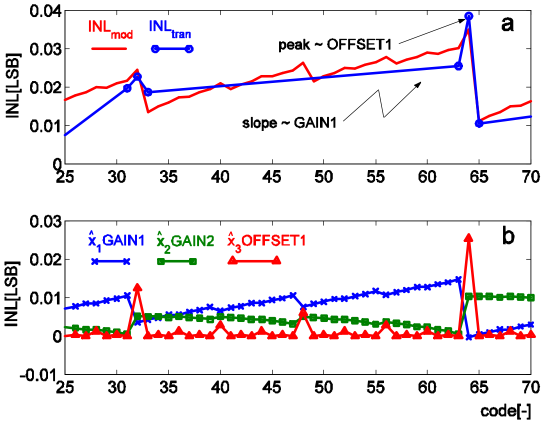

Fig. 5. Decomposition: a) model vs circuit performance, b) error components.

- Because of the existence of ambiguity groups, the number of error sources is much smaller than the number of ADC circuit instances and therefore the simulation time is significantly reduced.

- The ADC model tends to capture the “real” behavior of the transistor-level structure, since the error sources are assigned from the circuit design.

3.3. ADC Model Simulation and Verification

The next Design Evaluation step is the *model simulation*, analyzing the influence of individual error sources on the ADC INL characteristic. The error sources are joined into the groups following the ambiguity rule; for the subsequent modeling purpose it is advised to construct the ambiguity groups being linearly independent on each other. During the *model verification*, the *linear superposition principle* (valid under the assumptions given in IB) is checked for the sum of error sources attached to specific circuit instances:

$$INL\sum_{i=1}^{n} e_i\left(\sum_{c}\text{instance}\right)=\sum_{c}\sum_{i=1}^{n} INLe_i(\text{instance})+\Delta_{LIN} \qquad (1)$$

where n denotes the number of error sources, e_i is the magnitude of i-th error source, $INL\Sigma\ e_i$ is the INL contribution from a sum of n error sources, $INLe_i$ is the INL contribution from error source e_i, c is the selected set of instances and Δ_{LIN} is the difference from linearity, capturing also the interaction terms between error sources. Thanks to the behavioral level, a particular model simulation of a *full-code* INL pattern took less than one hour using the same environment as in Sec 3.1. This is more than 7600× less than if the full-code INL of the transistor-level design would be extracted. As a result of ambiguity group partitioning, three linearly independent groups exhibiting different patterns GAIN1, GAIN2 and OFFSET1 were found - see Fig. 4. Table 1 documents the overall shortage of the simulation time and modeling effort applying the proposed Design Evaluation approach. The transistor-level ADC design comprises more than 300 instances to examine their influence on the INL characteristic. Performing the identification procedure, this large set is reduced to 11 error sources caused by specific instances. Here, for example the

Table 1. Categorization of error sources.

Error source (root-causing instance)	Block	Ambiguity group
	Typ. Error level	INL_{max}

RIO(N1)
RIO(N2)
RIO(PN1)
	SI memory cell
	$2.8\cdot10^{-4}$
		GAIN1
		20 mLSB

GREF(INP)	*Input stage (INP)* *100 nS*	GAIN2 15 mLSB

LAMBDAREL(N1)
LAMBDAREL(N2)
LAMBDAREL(PN1)
	SI memory cell
	$15\cdot10^{-9}$	

VOS(K)	*Comparator (K)* *1.2 mV*	OFFSET1 50 mLSB

CHI(N1)
CHI(N2)
CHI(PN1)
	SI memory cell
	40 nA	

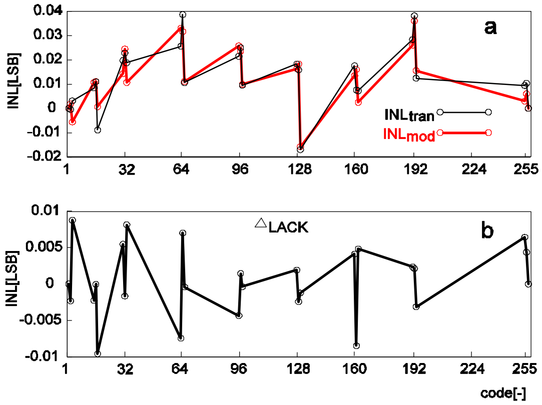

Fig. 6. Generalized architectural mapping: a) INL, b) lack-of-fit.

RIO(N1) denotes the INL contribution from the RIO error source of the N1 memory cell instance. Finally, there are only three groups of characteristic INL patterns as a result of the ambiguity rule partitioning. The model verification discipline proved that the maximum difference from linearity was in order of 10^{-4}. This makes the model derived directly suitable also for higher resolution algorithmic A/D converters.

3.4. Model-based ADC Design Streamlining

The last Design Evaluation step fits the extracted INL performance of the transistor-level ADC design (Fig. 3) into the behavioral model characterized by ambiguity groups of error sources (Fig. 4). This *decomposition* process can be described by the following equation:

$$INL_{tran} = \boldsymbol{A}_{mod}\,\hat{x} + \Delta_{LACK} \qquad (2)$$

In our case, the $INL_{tran} \in \Re^{27}$ is the extracted 27-point transistor-level ADC performance and $\boldsymbol{A}_{mod} = [e_1\ e_2\ e_3]$ is the 3×27 *model matrix* with columns representing error mechanisms, i.e. $e_1 = GAIN1$, $e_2 = GAIN2$, $e_3 = GAIN3$. The vector $\hat{x} = [\hat{x}_1\ \hat{x}_2\ \hat{x}_3]^T$ contains the decomposed model coefficients and $\Delta_{LACK} \in \Re^{27}$ is the *lack-of-fit* capturing the linearity difference and error mechanisms uncovered by the model. Being a part of (2), we can define the $\boldsymbol{A}_{mod}\hat{x}$ term as the INL_{mod} performance expressed by a weighted sum of error source ambiguity groups:

$$INL_{mod} = \hat{x}_1 GAIN1 + \hat{x}_2 GAIN2 + \hat{x}_3 OFFSET1 \qquad (3)$$

The decomposition described by (2) and (3) was numerically solved in MATLAB, gaining the model coefficients and the lack-of-fit which was proven to cover more than 50 per cent of error mechanisms present in the transistor-level circuit design. Inspecting the zoomed-in INL_{tran} characteristic (Fig. 5), the OFFSET1 ambiguity group can be determined by the height of the isolated peaks around the major transitions (Fig. 5a) whereas the GAIN1 group can be recognized as the slope of the interconnecting line between these transitions (Fig. 5b). *The root-cause identification rules stated above allow one to create a streamlining guidelines on the considered SI ADC structure.* For example the impact of SI memory cell charge injection and static comparator offset can be directly estimated from the statically measured INL characteristic as to calibrate the device under test. Conversely, the knowledge of the identical performance effect on CHI and VOS errors allows their concurrent optimization in the ADC circuit design. The typical circuit error levels extracted from the ADC design [5] and SI memory cell chip [6] are summarized in the middle column of Table 1. The last column of this table evaluates the INL contribution of each ambiguity group, indicating that the dominant one is in our case OFFSET1. Furthermore, we suggest some improvements on the finite model accuracy which is caused for example by the non-linear nature of the charge injection. A possible solution is to include a record of the extracted CHI pattern into the ADC model; however, the requirements on simulation time are expected to significantly increase. Another approach based on "generalized architectural mapping" was tried instead. The ADC architecture was enhanced by another error generating mechanisms, using the *bit error predictor*. It is a fictive block which contains the description of error sources belonging to the binary-weighted and segmented [4] SAR ADC architecture:

$$S\left(n_{bin}, n_{seg}\right) = 2^{-n}\left(\underbrace{\frac{2^{n} - 2^{nbin}}{2^{nseg} - 1}\sum_{i=0}^{2^{nseg}-2} W_i}_{segmented} + \underbrace{\sum_{i=0}^{nbin-1} B_i 2^{i}}_{binary-weighted}\right) \qquad (4)$$

Here, $n=8$ is the number of predictor bits (same as the ADC resolution), n_{bin} is the bit number of the binary-weighted fraction $n_{seg}=n-n_{bin}$ is the number of segmented bits, B_i are the binary-weighted bit values and W_i are the segmented bit values described by the function of a "thermometric" decoder [4]. Re-running the design decomposition process with a system of 15 error sources ($n_{bit}=4,\ n_{seg}=4$), a very good fitting result capturing 75 per cent of the INL_{tran} performance was achieved - see Fig. 6. However, the resulting model order is pretty high in comparison with the extracted 27-point INL_{tran} characteristic. This may indicate an improper model versus circuit correlation suggesting that the full-code prediction of the ADC characteristic can be incorrect. Despite this fact, the "generalized architectural mapping" is a possible way of further model refinement.

4. CONCLUSION

The main asset of this paper is the proposed concept of step-by-step Design Evaluation successfully documented on the SI algorithmic ADC structure. At this point, the main benefit are newly formulated root-cause identification rules suitable for direct design optimization, not achievable by using traditional testing approaches. Applying our methodology, the circuit imperfections of a real transistor-level ADC design can be directly estimated from the INL and DNL response as to calibrate or suppress them on a device under test. Moreover, the proposed approach can dramatically reduce the total time needed for design verification, as it was successfully demonstrated on our ADC example. The Design Evaluation rules described in this paper are generally suitable for the algorithmic class of data converters, since the whole procedure was developed on a generic system-level scheme. A possible continuation of this work is to extend its results into the field of production testing by fabrication of the ADC device samples and statistical processing of the measurement data.

ACKNOWLEDGMENTS

The results concerning the Switched-Current building blocks were achieved within the frame of co-operation between the Department of Circuit Theory Faculty of Electrical Engineering CTU Prague and ASICentrum Prague. The majority of research concerning data converter Design Evaluation was carried out at the Department of Microelectronic Engineering University College Cork. The work has been supported by the research program "Research in the Area of the Prospective Information and Navigation Technologies" No. MSM6840770014 of the Czech Technical University in Prague. The Switched-Current test chip design was sponsored by ASICentrum Prague, the research concerning data converter Design Evaluation was supported by Enterprise Ireland, Grant No. IP/2004/207.

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