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THE DATA FORMATS IN OPERATIONS PERFORMED IN MEASUREMENT OF DATA FROM ELECTRICAL POWER SYSTEM

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Abstract − The paper builds on the issues, contained in the another article [1] submitted to the XXI IMEKO World Congress concerning the data synchronization in process of measurement and registration of parameters characterizing the electrical power network. The paper discusses the formats of data in individual operations performed in instrument designed for analyzing and estimation of measured quantities.

Keywords: data format, synchronization, interface, power quality.

1. INTRODUCTION

The fluency of operations concerning the acquisition of analog samples of signals from electrical power network depends on the synchronization of operations performed in measurement and registration track. During these operations the data are repeatedly converted and transmitted between functional blocks of instrument [2].

The configuration of instrument, elaborated in Department of Marine Electrical Power Engineering of Gdynia Maritime University, is shown in Fig. 1. Main operations of instrument connected with calculation of parameters characterizing the electrical network power quality are performed in DSP (Digital Signal Processor).

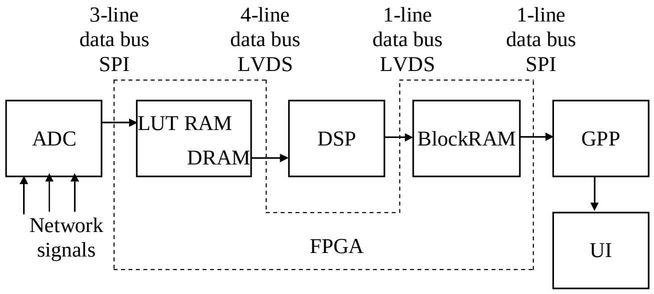

Fig.1. The configuration of the measurement and registration track of data from electrical network [1].

The samples of electrical network signals are delivered to DSP after their analog-to-digital (A/D) conversion into the digital representation in analog-to digital converter (ADC).
The values of parameters, obtained as a result of the calculations in DSP, are transmitted to general purpose processor (GPP). This processor together with its peripheral devices (graphical display and keyboard) serves as the user interface (UI). It is equipped also in Ethernet and USB ports. The direct links ADC-to-DSP as well as DSP-to-GPP can not be implemented because of different interface ports present at the communicating devices, both in the physical layer and the data link layer. All interfaces used for communication between the instrument functional blocks are synchronic serial links. Differences in physical layer are resulting from various standards of signals carrying the digital data, both in terms of the type of signals as well as parameters relating to amplitude and time. Also the clock signals operations, synchronizing the data sending and receiving, are different in these interfaces. Differences in the data link layer refer to the format of the basic data blocks transmitted using various interfaces and to the order of the individual bits in the frame.
The integrated circuit AD7656 from Analog Devices [3] has been selected and implemented in measurement track as the ADC. It contains three pairs of 16-bit analog-to-digital converters. Each of them can be independently initialized for A/D conversion of analog signals from two measurement channels. The digital data from these two converters are placed one by one in output buffer. The device is equipped with three output buffers, the separate buffer for each pair of converters. The data from the buffers can be outputted by means of three data lines in SPI (Serial Protocol Interface) standard, each connected to its buffer.

The processor ADSP TS-201 TigerSHARC from Analog Devices [4] serves as the DSP. It is equipped with LVDS (Low Voltage Differential Signaling) interface ports [5]. Two of them are used for communication with the measurement track other devices.

The processor LPC3250 (ARM9 family) [6], installed on development board phyCORE from NXP, fulfils the functions of GPP. Among others ports, it has SPI interface, used in measurement track for communication with DSP.

To establish the communication between main blocks of instrument (ADC, DSP and GPP) the FPGA device was applied. Its functions are fulfilled by XCS1000 Xilinx Spartan 3 [7]. It enables the proper data flow between considered blocks of instrument and ensures the connection between different interface ports as well in physical as data link layers.

The data link between ADC and FPGA is controlled by the clock generated in FPGA, as well as the data transmission from FPGA to DSP is synchronized by the FPGA clock. The data sending from DSP to FPGA is controlled by the DSP clock, while the transmission from FPGA to GPP is carried out under GPP clock control.

The paper is organized as follows. The basic resources of FPGA, used to establish the connections between main functional blocks of instrument are shortly discussed. The formats of data in operations related to data transmission from ADC via FPGA to DSP are presented. The formats of data sent from DSP to GPP, after processing in DSP, also via FPGA, are shown. Finally, the conclusions are drawn.

2. THE FPGA RESOUCES USE IN DATA TRANSFER IN INSTRUMENT

The FPGA performs important role in measurement track of instrument enabling connections between main functional blocks. The FPGA is equipped with basic elements IOB (Input/Output Block) blocks, implementing the input and output functions of an FPGA. They can be configured to meet, in physical layer, the requirements of a few standards of interface ports. Among others, IOBs are capable to be configured to comply with the standards of interfaces implemented in ADC, DSP as well as in GPP.

To customize the data link layer functions and to keep the data flow between different interfaces, the formats of data must be changed in FPGA. In these operations the main functions are fulfilled by two types of FPGA elements: LUT RAMs and Block RAMs.

Inside each of a configurable logic block (CLB) of FPGA is a look-up table (LUT) element. It is normally used for logic functions, but it can be reconfigured as RAM which can accommodate 16 bits. They can be combined into a larger RAM. This is DRAM - distributed RAM.

Another kind of memory, present in FPGA, is the Block RAM. It is a dedicated two-port memory containing several kb of RAM. Typical FPGA contains at least a few such blocks. It is possible to use both single port as well as dual port Block RAMs. In dual port Block RAMs both the ports operate at different clock speeds. The DRAMs can work without any latency, while the Block RAMs have a minimum latency of 1 clock cycle.

3. DATA FORMATS IN OPERATIONS BETWEEN ADC AND DSP

In Fig. 2 the format of data collected in ADC buffers as a result of A/D conversion of samples from three channels measuring the 3-phase network voltages is shown. After the end of A/D conversion of the current set of samples, the 16-bit words are ready to simultaneous readout on three lines in SPI standard. The data outputting is done under control of the clock generated in FPGA. The order of bits in words collected in ADC buffers words is shown in Fig. 2. As the first are sent out the most significant bits (MSB), respectively: A15, B15 and C15. The transmission takes 16 cycles of control clock. The sequence and timing relationships of bits sent in relation to the control clock signal are shown in Fig. 3 (for one data line).

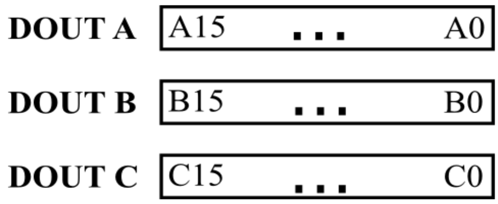

Fig.2. The format of data collected in ADC buffers, ready to send via SPI interface.

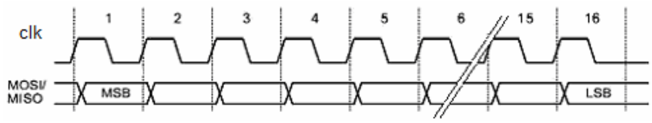

Fig.3. The timing in data transmission from ADC to LUT RAM in FPGA.

The data frames are transferred from ADC to FPGA buffers, namely to the LUT RAM buffers. The order of bits stored in LUT RAM buffers is shown in Fig. 4. The buffers are organized as the FIFO (First In, First Out) shift registers, where first bit saved in buffer goes out first (respectively: A15, B15 and C15).

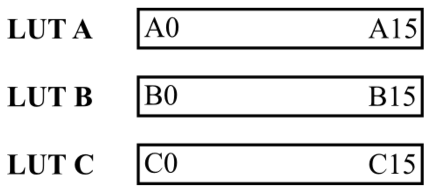

Fig.4. The order of data written to LUT RAM in FPGA.

The data for transmission to DSP must be contained in 128-bit frames, so they have to be re-organized and placed in another part of FPGA. Because each digital representation of set of analog samples is separately sent to DSP, the LUT RAM content is moved to the set of DRAM blocks. The data are sequentially outputted from registers, in following order: firstly from LUT A, next from LUT C and finally from LUT B.

The operation of data transfer from LUT RAMs to DRAMs is controlled by two synchronized clocks (Fig. 5). First of them, clk_L, controls the outputting of data from LUT RAMs, and second, clk_D, manages the writing of individual bits to DRAM P and DRAM N memory blocks. The frequency of clk_L is twice the frequency of clk_D. The entry to DRAM P is controlled by rising edge of clk_D, while the access to DRAM N takes place for falling edge of clk_D clock. The capacity of each DRAM is 64 bits. The order of subsequent bits located in both DRAMs is shown in Fig. 6. This way the data in volume of 2x24 bits representing samples are segregated to be ready for transmission to DSP via 4-wire LVDS interface.

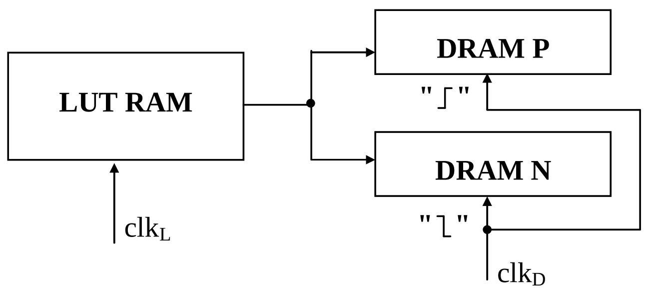

Fig.5. The control of data transfer to DRAM.

When the transfer from LUT RAM is completed, the other FPGA clock is initialized. This clock controls the communication with DSP. For each edge of clock the data are fetched in fours from one of DRAMs, for rising edge of clock from DRAM P and for falling edge – from DRAM N. The multiplexer (Fig. 6) directs the data from DRAMs to the IOB blocks, alternately from DRAM P and DRAM N. In one cycle of control clock two memory rows are fetched, first - consisting of four bits from DRAM P and second - four bits from DRAM N. The bits of each column, numbered from 1 to 4 (Fig.6), are fed sequentially to the LVDS line marked with the same digit as the column. The IOBs in the output of multiplexer form the 4-wire port LVDS, from where each data bit is transmitted using two differential lines (labeled in Fig. 6 as “+” and “-“).

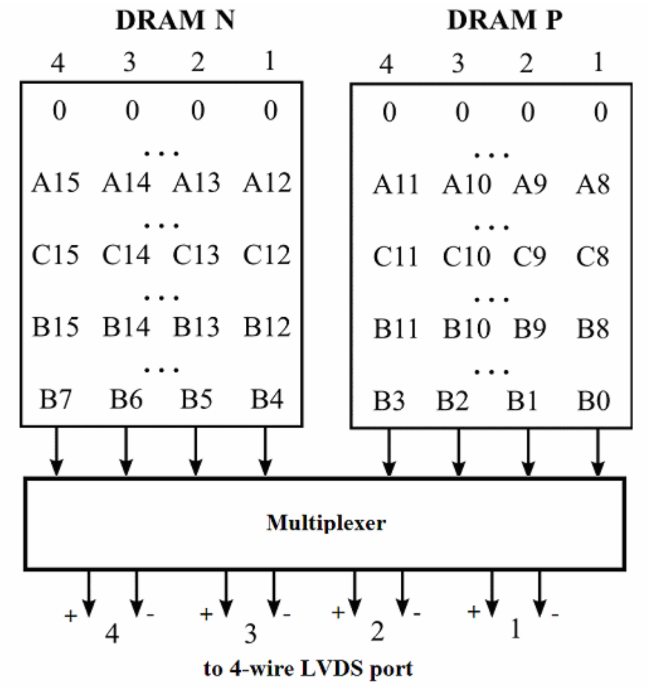

Fig.6. The format of data stored in DRAM in FPGA.

The frame transmitted to DSP via LVDS interface consists of 128 bits (quad word). The order of bits in the frame is shown in Fig. 7. The data representing samples taken by ADC are located on positions from 0 to 47. The remaining part of frame is filled with zeros.

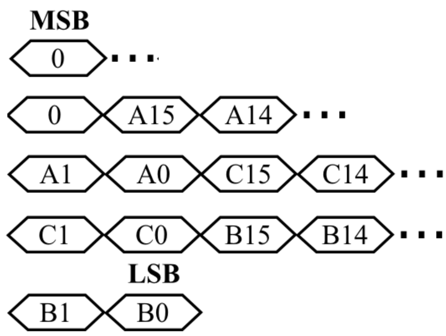

Fig.7. The format of data frame sent from FPGA to DSP.

In the 4-wire LVDS interface the 128-bit frame can be transferred in 16 clock cycles. For each edge of the clock four bits are sent simultaneously. The succession of bits transferred via 4-wire LVDS to DSP is shown in Fig. 8.

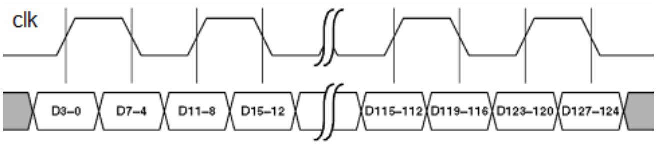

Fig.8. The sequence of data in 4-wire LVDS in data transmission from FPGA to DSP [4].

All these operations meet the requirements for the expected rate of data acquisition the from electrical power network, i.e. sampling of three-phase voltages at a rate of more than 200 kS/s and the fluent data processing.

4. FORMATS OF DATA FRAMES IN TRANSMISSION BETWEEN DSP AND GPP

While the frames sent from ADC to DSP contain the digital representation of set of samples taken at the same moment in time, the data transmitted from DSP to GPP include the parameters calculated on the base of collected samples or simply the data representing collected samples. The data in DSP are accumulated in 4 kB blocks. During the transfer to Block RAM in FPGA via 1-wire LVDS link the data are divided into 32 frames, each of them contain 128 bits of data. The sequence of bits in the frame is shown in Fig. 9. The transmission of one frame takes 64 clock cycles. The clock signal controlling the communication from DSP to Block RAM in FPGA is generated in DSP.

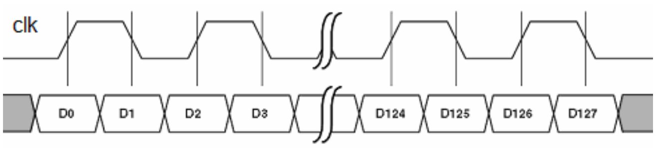

Fig.9. The sequence of data in 1-wire LVDS in data transmission from FPGA to DSP [4].

The LVDS interface port in FPGA is configured as in previous part of measurement track using IOB blocks.

The single Block RAM in FPGA applied in instrument contains 2 kB memory cells, so two Block RAMs are used for recording of 4 kB data block (Fig. 10).

Because the data from DSP via LVDS are transferred in tact of both edges of control clock, the entry to the Block RAM has to be performed also for both edges of the clock. It's the second reason why two Block RAMs are used: the data are saved to the first for rising edge of control clock and for its falling edge - to the second. The order of the data saved in both memory blocks is shown in Fig. 10.

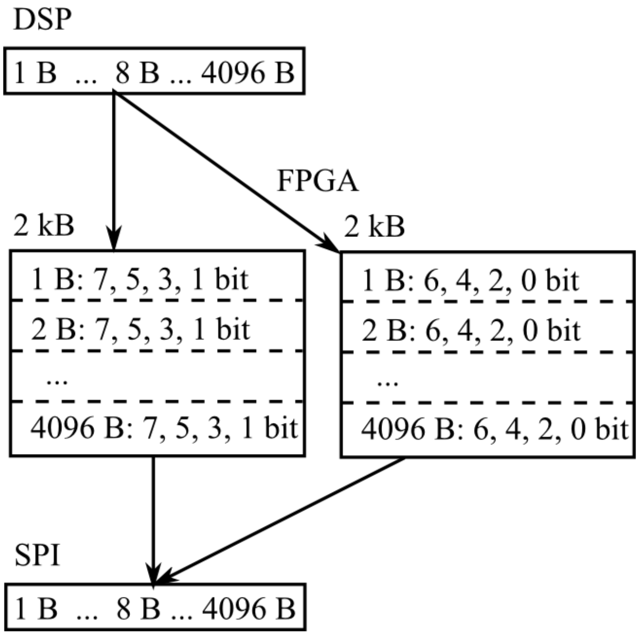

Fig.10. The flow of data from DSP to FPGA Block RAM and next to GPP.

Each of 2 kB Block RAMs is implemented as a dual port Block RAM. It means that the access to the memory cells can be arranged using two independent ports with two separated sets of data and address lines. First port is used for data transfer from DSP to Block RAM and second – for data readout and transfer to SPI interface register located in another part of FPGA.

Fig. 10 shows the order of data sent to GPP in 8-bit frames via SPI interface. The clock signal generated in GPP controls all operations connected with data transmission, i.e. the sequential addressing of the cells of Block RAMs and serial sending bits of each byte to SPI port in GPP.

The proper synchronization of the operations performed in the data measurement and registration track is essential to fulfill the assumed measurement functions. For the integrated circuits, selected to perform the functions of ADC, DSP and GPP as the major functional blocks, the FPGA implementation is crucial for the successful design of the elaborated measuring instrument.

5. CONCLUSIONS

Ensuring the correct transmission of data between functional blocks of instrument requires performing of many operations connected with data manipulation.

Numerous changes of data formats in measurement track must be performed without any errors and excessive delays in order to maintain the system proper operations.

It is necessary to precisely control the format of the data in individual operations. Otherwise, the fluency of the data flow in system is not to obtain.

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