

## Design of a $1 \mu s$ real-time low-noise data acquisition for power converters control loop

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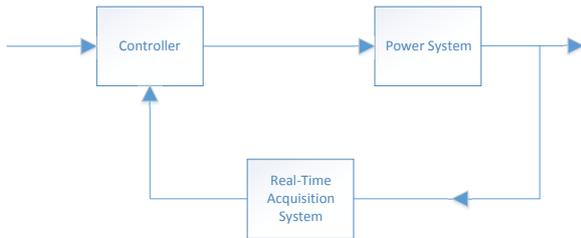


Fig. 1. Basic Diagram of a Control System

**Abstract** - The proof of principle of a real-time data acquisition system to be integrated into a digital control loop for controlling the power converters of the Compact Linear Collider is presented. The system is based on an ultra low noise analogue front-end with  $1.1 \text{ ppm RMS}$  noise (referred to input), and about  $1 \mu s$  of real-time delay. After the analogue conditioning, a fully-differential analogue-to-digital converter is foreseen. The requirements of this system, directly derived from the accelerator performance, are discussed and translated into design specification. The results obtained by means of Pspice simulations are reported in order to prove that the design is feasible with the proposed architecture. Finally, the results of the experimental validation of the prototype, currently under design, will be included in the final paper.

**Keywords:** Power Converters, Linear Accelerators, Data Acquisition System, Real-Time Systems

### 1. INTRODUCTION

Real-time acquisition systems [1] have been focus of scientific interest in different fields, from medical [2] to military applications [3]. In their design, the main challenges arise from satisfying simultaneously the metrological requirements and the time constraints imposed by the specific application. One of the most demanding real-time applications is represented by the control for power converters, in order to check the power quality and eventually correct non-repeatability errors [4]. In this type of digital control loops, (Fig.1), the data acquisition system provides the so-called *actuating variables* to be sent to the controller inside a direct digital control. High-level metrological challenges for real-time data acquisition design are arising more and more at CERN, from the

new linear electron-positron particle accelerator currently under study, the Compact Linear Collider (*CLIC*) [5]. Its combination of high-energy and experimental precision will allow collisions up to several TeV, exploring energy regions never reached before. In order to reach the desired energy level, together with a reasonable power consumption from the electrical grid, *CLIC* power converters [6] are demanded to deliver a pulsed power repeatable in the order of few tens of ppm [7]. To do that, a high-voltage modulator is currently under design by the lab for high-power electronics system at *ETH Zurich (CH)* [8] and the *LEEPCI* lab at Laval university (CA) [9]. The latest topology of the *ETH* design is depicted in Fig.2. The modulator is composed of a charging system which accumulates energy from the grid obtaining a stable  $3 \text{ kV}$  output voltage. The switching unit allows the stored energy to be released during  $140 \mu s$ , obtaining a pulse train on the primary side of a split-core transformer. The voltage output of the charging system is regulated by an active bouncer for mitigating the effect of discharge of the capacitors bank during the pulses. Finally, on the secondary side, the pulses are amplified up to  $180 \text{ kV}$  directly feeding the klystrons. A high-voltage divider [10] is used to convert the  $3 \text{ kV}$  voltage into  $10 \text{ V}$  in order to be handled by a suitable real-time digitizing system. In this context, the system measures and provides a suitable adjustment value for the switching unit input voltage, namely a  $3 \text{ kV}_{DC}$  with a superposed ripple within a maximum real-time delay of  $1 \mu s$ . In this paper, the design of the real-time measurement system is proposed. It is composed by a  $1.1 \text{ ppm RMS}$  noise analogue front-end for signal conditioning and a fully-differential ADC. In section 2, the requirements of this measurement system are reported and discussed while in section 3, the proposed architecture is presented, by detailing both the concept and the physical design. In section 4, the results obtained by means of Pspice simulations are presented to demonstrate that the proposed system meets the stated requirements. In the final paper, the results of the experimental validation of the prototype currently under design for the power converter system of *CLIC* will be illustrated.

### 2. REQUIREMENTS

In a real-time control of power converters for the last generation of particle accelerators, a digital control loop is exploited to guarantee the requested performance of the

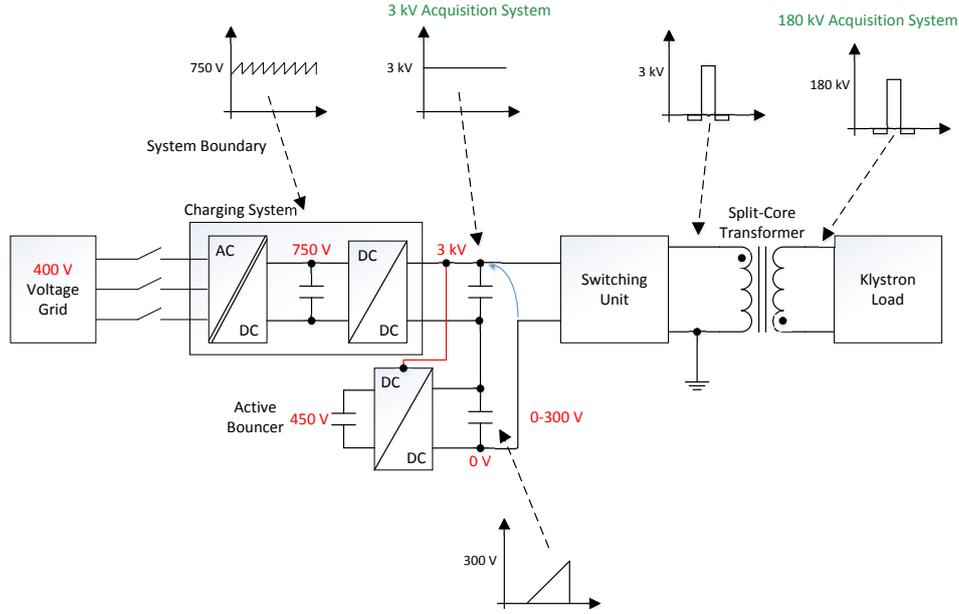


Fig. 2. Topology of the High-Voltage Modulator under design at ETH Zurich

power system. In this section, the requirements of the real-time measurement sub-system for the primary side control loop (3 kV Acquisition System in Fig.2) are discussed.

### 2.1. Sampling Frequency and Bandwidth

Depending on the control loop frequency, the measurement system should deliver one sample for each loop period defining a sampling frequency ( $f_s$ ) equal to the loop frequency. Directly deriving from the sampling frequency, the analogue bandwidth should be chosen accordingly to Nyquist-Shannon sampling theorem. Any spectral component higher than  $f_s/2$  should be, in principle, cut-off in order not to produce any aliasing on the digitized signal. Consequently, the analogue bandwidth should be less than  $f_s/2$  and guarantee enough attenuation from  $f_s/2$  on. For CLIC, a loop frequency of 600 kHz is foreseen, accordingly defining (i)  $f_s = 600$  kS/s and (ii) an analogue bandwidth  $< 300$  kHz.

### 2.2. Repeatability and Noise

The real-time measurement system will be used to correct non-repeatability errors in the order of 50 ppm of full-scale. The particular application, discussed in [11], defines the Pulse-to-Pulse Repeatability (PPR) as:

$$PPR = \max|V_{i,j} - V_{i,j+1}| \quad (1)$$

where  $V_{i,j}$  and  $V_{i,j+1}$  are the instantaneous voltage values in the “same” (in equivalent time) sampling instant  $i$  between two consecutive pulses on the secondary side of the modulator, namely  $j^{th}$  and  $j^{th} + 1$  (Fig.3).

To be able to properly measure and correct variations of 50 ppm, the system should have enough precision for appreciating them. In addition, it has been studied in [11] that if the instrument has a suitable stability within the pulses

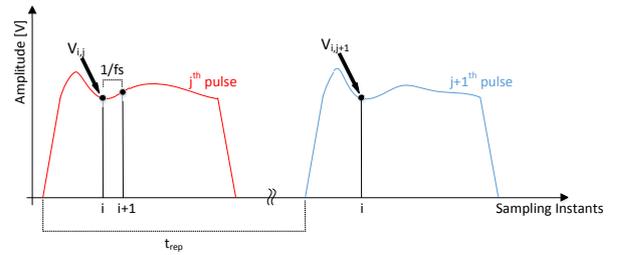


Fig. 3. Pulse-to-Pulse Repeatability Definition.

period, the noise is the only factor affecting repeatability, thus all long term effects can be neglected (e.g. temperature drift). In this case there is a strict relation between the RMS value of the instrument noise ( $\sigma$ ) and the PPR level of the instrument itself. In [12], the statistical distribution of PPR was studied and demonstrated to be accurately described by equation 2:

$$f_{PPR}(z) = \begin{cases} 2N_s f_{Y_i}(z) [2F_{Y_i}(z) - 1]^{N_s-1}, & z \geq 0 \\ 0, & z < 0 \end{cases} \quad (2)$$

where  $N_s$  is the number of samples acquired within the Pulse Duration  $PD$  of 140  $\mu$ s. By assuming that the instrument is affected by an Additive White Gaussian Noise AWGN,  $f_{Y_i}$  and  $F_{Y_i}$  are respectively the pdf and the cdf of a normal random process, thus  $f_{PPR}$  only depends on  $\sigma$  and  $N_s$ . Once the sampling rate  $SR$  is fixed, the number of samples to be acquired can be calculated as  $N_s = PD \times SR$  and, in turn, the mode of the uni-modal PPR distribution can be estimated as  $M = 3.32 \times \sigma$ . In this context, in order to properly measure and correct non-repeatability errors in the order of 50 ppm, the maximum allowed instrument repeatability level can be chosen in terms of confidence level.

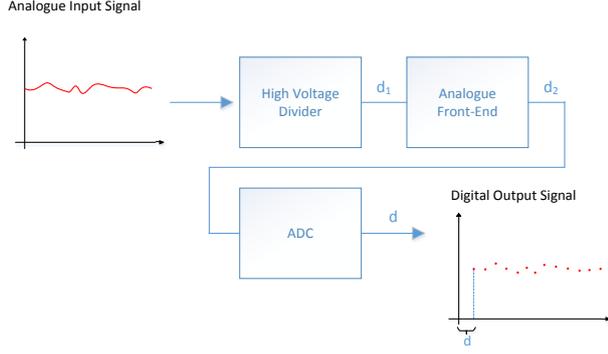


Fig. 4. Definition of Delay in a Power Converter Real-time Data Acquisition

Table 1. Main Requirements

Parameter	Symbol	Value
Repeatability	$Rep$	$< 35 \text{ ppm}$
RMS Noise	$\sigma$	$< 10.5 \text{ ppm}$
Sampling Frequency	$f_s$	$600 \text{ kS/s}$
Bandwidth	$BW$	$< 300 \text{ kHz}$
Delay	$d$	$< 1 \mu\text{s}$

For instance, if a confidence level of 99.9 % is chosen, a value of  $M = 35 \text{ ppm}$  can be identified as the instrument target repeatability. By reversing the relation that links the mode of repeatability to the instrument noise, the maximum RMS noise level can be calculated to be  $\sigma = 10.5 \text{ ppm}$ .

### 2.3. Delay

Delay is one of the most important parameters of a control loop; indeed, delays could jeopardize the stability of the loop itself. For this system, a delay  $d < 1 \mu\text{s}$  is specified. This is a challenging specification if combined with an analogue bandwidth of less than  $300 \text{ kHz}$ , as required by CLIC application. Indeed, by only considering a simple 1<sup>st</sup> order filter at  $300 \text{ kHz}$ , a delay of  $\frac{1}{2\pi \cdot 300 \text{ kHz}} \approx 530 \text{ ns}$  will be introduced. In Fig.4, all the contributions which have to be taken into account are sketched.

For the sake of simplicity, all the parameters of the requirements for the real-time measurement system are summarized in Table 1.

## 3. DESIGN

In this section, the design choices of the analogue front-end are discussed with respect to the defined requirements.

### 3.1. Concept Design

The  $3 \text{ kV}$  voltage is reduced to  $10 \text{ V}$  by means of a high-voltage divider. At this point, a reference  $10 V_{DC}$  is subtracted from the original signal in order to center the signal around zero and then amplify only the superposed ripple by a factor  $G$  to best fit the ADC range (the instrument will be equipped with both an embedded voltage reference and a connector in order to use an external reference). By specification from ETHz, a maximum ripple of  $\pm 100 \text{ mV}$

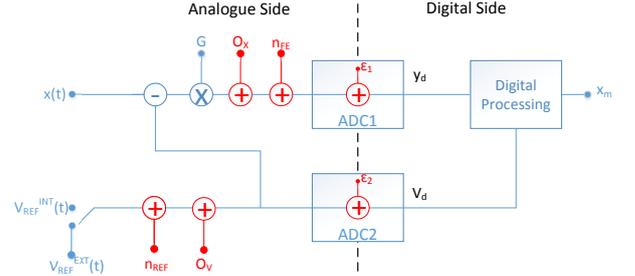


Fig. 5. Measurement System Block Diagram

is expected after the filtering effect of the active bouncer on the charging system output. Thus, an amplification  $G = 20 \text{ V/V}$  is used in order to let the output signal vary between  $\pm 2 \text{ V}$ . Down-stream of these two operations, an unwanted offset ( $O_x$  in Fig.5) will be introduced due to all the possible analogue components as well as a gain error. This is faced by digital processing in order to properly reconstruct the original signal. Finally, a switch allows to connect an external  $10 V_{DC}$  reference, ( $V_{REF}^{EXT}$ ) for a direct calibration of the internal generated reference  $V_{REF}^{INT}$ .

During normal working conditions, both the conditioned signal (affected by the front-end noise  $n_{FE}$ ) and the internal reference DC voltage (with a superposed noise  $n_{REF}$ ) have to be acquired by two ADCs obtaining the digitized signals  $y_d$  and  $V_d$  (Fig.5). These two signals will be affected by the quantization errors of the two ADCs, respectively  $\epsilon_1$  and  $\epsilon_2$ .

Thus, particular care should be posed into:

- accurately measure gain and offset for proper compensation (an effective strategy will be studied)
- realize a very low-noise front-end in order to keep  $n_{FE}$  as low as possible
- heavily filter  $V_{REF}$  to reduce  $n_{REF}$
- use high-resolution ADCs to keep both  $\epsilon_1$  and  $\epsilon_2$  as low as possible

### 3.2. ADC Noise vs Analogue Noise

By assuming good gain and offset compensation, the quality of the reconstruction of  $x$  depends on both the analogue noise ( $n_{FE}$  and  $n_{REF}$ ) and the digital noise ( $\epsilon_1$  and  $\epsilon_2$ ). In this early stage, the ADCs noise can be simply derived by their ENOB specification.  $\epsilon_1$  is the noise of ADC1 which has to digitize the conditioned signal. On the AD7625 datasheet a Signal-to-Noise-And-Distortion ratio (SINAD) of  $92 \text{ dB}$  is specified. Equation 3 allows the Effective Number Of Bits (ENOB) to be calculated as:

$$ENOB = \frac{SINAD - 1.76}{6.02} \approx 14.9 \quad (3)$$

Moreover, down-stream of the subtraction and amplification operations, the signal to be measured varies in the range

$\pm 2 V$ , thus the expected *RMS* noise Referred to Input (*RTI*) can be obtained.

$$\begin{aligned}\epsilon_1 &\approx \frac{Q}{\sqrt{12}} = \frac{4}{\sqrt{12} \cdot 2^{ENOB}} \approx 35.5 \mu V = \\ &= \frac{35.5 \mu V}{G \cdot 10 \mu V} \approx 0.17 \text{ ppm}\end{aligned}\quad (4)$$

with  $Q$  being the LSB. In this case, the *RMS* value of the  $ADC_1$  noise is expected to be comfortably lower than the noise specification defined in section 2. On the lower branch,  $\epsilon_2$  is the noise of  $ADC_2$ , which has to digitize a  $10 V_{DC}$  voltage, thus an ADC with an appropriate full-scale should be chosen. As an example, the  $AD7610$  has a Signal-to-Noise-And-Distortion ratio (*SINAD*) of  $93 \text{ dB}$  when working with a full-scale range of  $0 - 10 V$ . This allows calculating its *ENOB* to be  $\approx 15.2$  by means of equation 3 and, consequently, the expected *RMS* noise to be  $\approx 7.7 \text{ ppm}$ . In this case,  $\epsilon_2$  is comparable with the *RMS* noise specification defined in section 2. However,  $\epsilon_2$  can be heavily reduced by exploiting oversampling and filtering techniques [13]. In fact, the real-time requirements are only specified for the upper branch of the diagram sketched in Fig.5, thus a completely independent sampling and processing strategy can be adopted for the  $V_{REF}$ . As an example, if  $\epsilon_2$  has to be reduced down to a given value  $k$ , an oversampling and averaging (by a factor  $N$ ) technique could be used, obtaining  $\frac{\epsilon_2}{\sqrt{N}} = k$ .  $n_{REF}$  is the noise coming from the *DC* reference voltage to be subtracted from the original signal. Since no bandwidth is required for this branch of the front-end, this voltage can be heavily filtered (for example down to  $20 \text{ Hz}$ ) in order to reduce it. Finally,  $n_{FE}$  is expected to be the main contribution to the overall noise. Indeed, a low-noise solution for the front-end was the main design constraint.

### 3.3. Physical Design

In Fig.6, the schematic of the proposed measurement system (analogue side) is depicted. On the upper branch, a switch allows selecting either the external or internal reference voltage. The internal reference voltage ( $V_{ref}^{INT}$ ) is obtained by means of the Linear Technologies voltage reference  $LT1236$  which delivers a very stable and low-noise  $10 V_{DC}$  voltage. The low-pass filter  $R_1C_1$  is tuned at about  $20 \text{ Hz}$  to heavily filter the reference voltage in order to keep  $n_{REF}$  as low as possible. The operational amplifier  $ADA4898$  in unity-gain buffer configuration is used to show a high input impedance in order not to affect the working conditions of the up-stream voltage divider. On the lower branch, a  $2^{nd}$  order low-pass filter ( $R_2C_2R_3C_3$ ) is used to cut the out-bandwidth noise off. This is the first stage of the anti-aliasing filter realized in this design. The cascade of two  $ADA4898$  in super-diode configuration realizes a very sharp clipping circuit to protect the input stage of the ADC [14]. In fact, if an unwanted over-voltage (either positive or negative) is detected at the input stage of the analogue front-end, the clipping circuitry cuts the over-voltage above two given thresholds ( $V_{clip+}$  and

$V_{clip-}$ ) and avoids that the differential stage amplification brings the signal out of the ADC range. At this point, both the reference voltage and the input signal have been handled by the input stage (filtered, buffered and eventually clipped). A Fully Differential Amplifier (model  $THS4532$ ) performs the subtraction of the reference *DC* voltage from the input signal and amplifies the resulting difference by a factor  $G = 20$ . The resistor network  $RN_1$ , highlighted in red in Fig.6, is the Vishay  $SMNz$ . It is composed by 4 matched resistors with (i) low relative tolerances ( $0.01 \%$ ) and (ii) low temperature coefficient ( $0.1 \text{ ppm}/^\circ\text{C}$ ). These characteristics are very important in this design in order to fulfill the hypothesis, stated in 2.2, that all the long term effects can be neglected and noise is the only factor affecting repeatability, in fact:

- Their ratio keeps constant while temperature changes (they are matched), allowing the gain and offset drift to be heavily reduced.
- They avoid degradation of *CMRR* due to unbalances of the two branches of the difference amplifier [15].

Finally the output filters  $R_7C_4$  and  $R_8C_5$ , together with the capacitor  $C_6$  add the  $3^{rd}$  pole to the embedded anti-aliasing filter obtaining about  $6 \text{ dB}$  of attenuation at  $300 \text{ kHz}$ . Indeed there is a trade-off between the desired analogue bandwidth (and, thus, the anti-aliasing effectiveness) and the corresponding delay which has to be minimized. In this design, the attenuation at  $300 \text{ kHz}$  was sacrificed in order to obtain an acceptable delay.

## 4. NUMERICAL RESULTS

In this last section, the requirements stated in section 2 are demonstrated to be achievable by the proposed architecture.

### 4.1. Noise and Repeatability

The noise introduced by the analogue front-end was estimated by means of the first Pspice simulation. The contributions of all the components sketched in Fig.6 are taken into account and the result, depicted in Fig.7, represents the *RMS* noise value referred to input (*RTI*) and expressed in ppm of full-scale. This simulation clearly indicates that the analogue noise to be expected by the circuit is comfortably lower than the stated requirement of  $10.5 \text{ ppm}$ . In fact, in Fig.7 the noise is estimated to be around  $1.1 \text{ ppm}$ . In [16], was demonstrated that if (i) the ADC does not saturate during the sampling, and (ii) the noise of the analogue front-end has a standard deviation greater than  $0.4\epsilon_1$ , the overall noise can be accurately modeled as Gaussian Noise (*GN*) as hypothesized in 2.2. In addition, in [12] was demonstrated that an instrument affected by a *GN*  $\sigma$ , is expected to have the mode of the *PPR* distribution equal to  $3.32 \times \sigma$ . Thus, in this case, the instrument is expected to show a repeatability level of about  $3.65 \text{ ppm}$ , almost 10 times better than the required one.

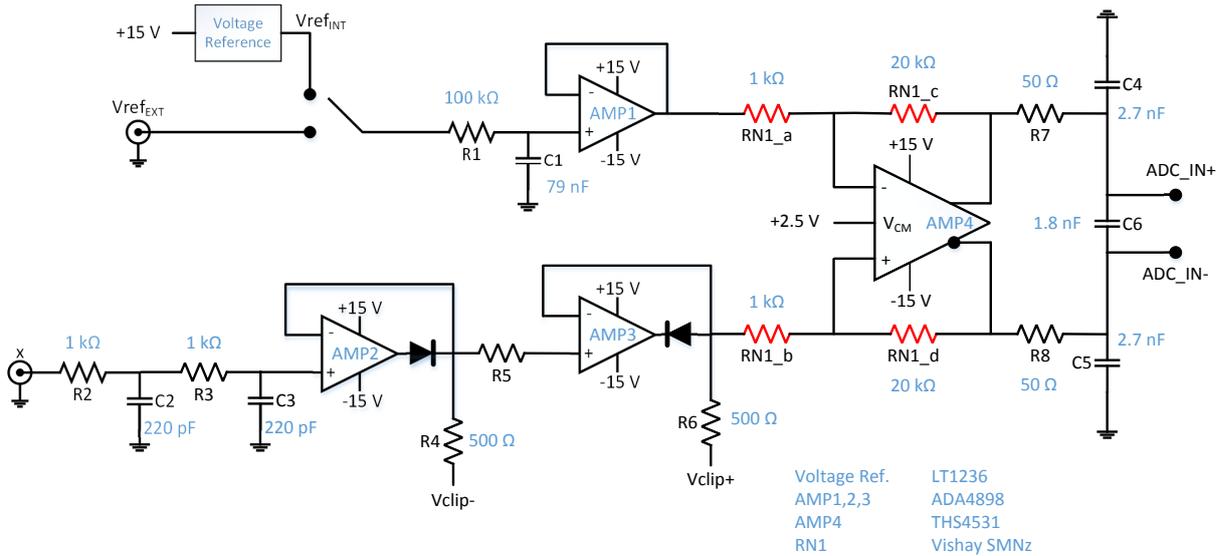


Fig. 6. Measurement System Schematic

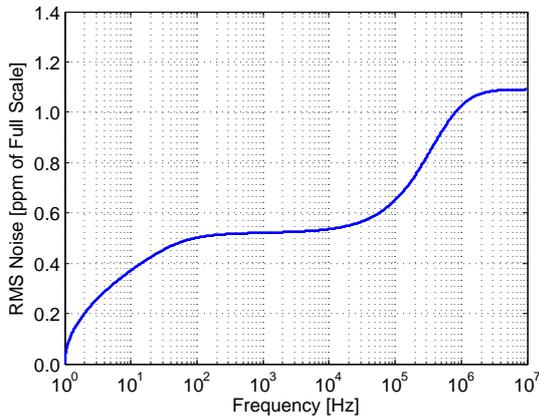


Fig. 7. Rms Noise of the Analogue Front-End

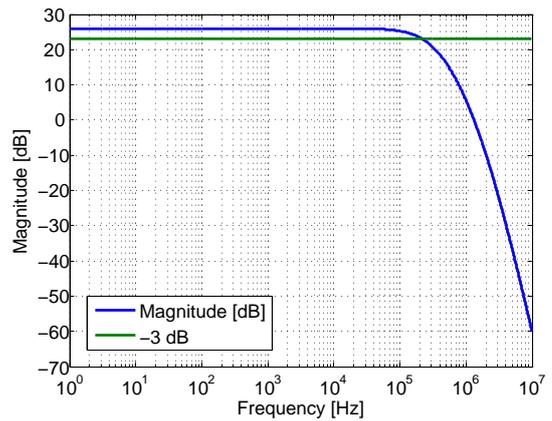


Fig. 8. Magnitude Bode Diagram

#### 4.2. Bandwidth

Another Pspice simulation was performed to verify the  $-3$  dB bandwidth of the proposed instrument. In Fig.8, the simulation result is depicted showing that the  $-3$  dB point is located around  $220$  kHz while an attenuation of about  $6$  dB is obtained at  $300$  kHz as set in 3.3.

#### 4.3. Delay

The last parameter to be verified is delay. A small-amplitude input step with  $10$  ns rise-time is given as input to the analogue front-end and the corresponding output signal is measured (the small amplitude is required in order not to activate the clipping circuit). In order to be directly comparable, in Fig.9, the input step was scaled (translated around zero and then amplified). As shown, the delay caused by the analogue front-end is estimated to be around  $900$  ns. In conclusion, the delay is lower than the requirement of  $1$   $\mu$ s. However, all the other contributions sketched in Fig.4 have to be considered. As an example, considering the

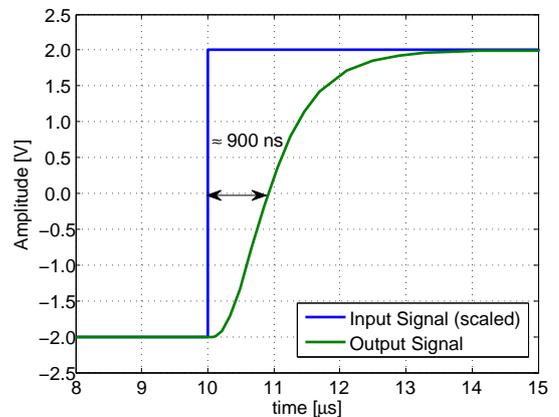


Fig. 9. Delay Introduced by the Analogue Front-End

*AD7625 ADC* an additional acquisition delay of 40 ns should be taken into account, as declared on its datasheet. This means that an allowable delay of about 60 ns is left for the voltage divider. However, the up-stream voltage divider will introduce a higher frequency pole into the signal path. This means that the filters of the analogue front-end might be tuned at higher frequencies with respect to the one considered in section 3, in order to respect the delay constraint.

## 5. CONCLUSIONS

The design and the proof of principle of a high-repeatability measurement system for controlling the high-voltage of the pulsed power converters of *CLIC* has been presented. The requirements of the system have been discussed together with the main design choices. Pspice simulations were performed in order to demonstrate the effectiveness of the proposed architecture. In particular, while bandwidth and noise were demonstrated to be comfortably achievable, the delay requirement turned out to be very challenging. The future steps of this research work are to thoroughly study the impact of the *ADC*, also regarding the choice of an adequate data communication protocol to be used. Moreover, a first prototype is expected to be produced soon in order to confirm the performance already assessed in simulation.

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