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# METROLOGICAL CHARACTERIZATION OF AN ENHANCED FAST DIGITAL INTEGRATOR FOR MAGNETIC MEASUREMENTS

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***Abstract*** **–** The pre-series of the last generation of fast digital integrators for magnetic measurements, the e-FDI, aimed at satisfying the more challenging requirements expected in the future, has been just developed and made available at CERN. The enhanced instrument improves the state of the art thanks to a high-performance analogue front-end, a new hardware for self-calibration, a finer time base speeding-up internal DSP operation, and a new peripheral bus controller for higher data throughput. The e-FDI is now undergoing the performance assessment tests and the metrological characterization. In this paper, after a short description of the e-FDI, main preliminary test results are reported and discussed.

***Keywords***: magnetic measurements, digital integrator, self-calibration, metrological characterization, peripheral bus interface.

## 1. INTRODUCTION

In particle accelerators, magnetic measurements require customized transducers and voltage integrators with state-of-art accuracy, measurement time, and data throughput. The on-field experience grown in the last decades has boosted up the design of new transducers and the utilization of dedicated digital integrator instruments to condition, process, and transfer the measured data. Nowadays, a primary role is played by the Fast Digital Integrator (FDI) [1], employed in the majority of magnetic measurement [2] even in superconducting cable testing [3], and marketed as FDI 2056 [4] by the Swiss company Metrolab under license from CERN and University of Sannio. Furthermore, the ongoing research effort produced an enhanced version of the instrument (e-FDI) [5], which should satisfy more challenging requirements expected in the future.

The design of e-FDI is largely inspired to the existing FDI [6]-[10] and improves the latter thanks to a new analogue front-end, a new hardware for accurate self-calibration, a finer time base, a better exploitation of the available on board processing capabilities, and a new controller for the peripheral bus interface. In fact, e-FDI front-end includes more configurability options in the choice of input impedance, attenuation by means of dividers, and amplifier gain. It also grants high performance in terms of distortion and noise rejection capability. The self-calibration hardware uses a couple of 20-bit DACs mounted in a differential configuration to realize a high-resolution DC calibrator, and substitutes the resistive network employed by FDI. The higher-frequency time base improves the accuracy of integration and speeds up the on-board DSP. The DSP in addition to the offset and gain error compensation and the digital integration, also performs all operations needed to configure the internal dual DAC calibrator and carry out the self-calibration procedure. Finally, the peripheral interface control strategy, involving direct memory access, allows a substantial increment of the data throughput, which is of interest when the external data collector has to retrieve data from several instruments having at disposal time slots of short duration.

In this paper, after a short remind of the main functional blocks of the e-FDI, the preliminary experiments required by the metrological characterization [6] are reported and the related results are discussed.

## 2. ENHANCED FDI FUNCTIONAL BLOCKS

The architecture of the e-FDI instrument is hosted on a single board including: an analogue front end, an 18-bit ADC sampling at a maximum rate of 500 kS/s, a digital circuit for self-calibration, a DSP for on-board processing, a control unit in charge of basic control operations as well as data routing, and a peripheral interface to send data to external devices (Fig. 1).

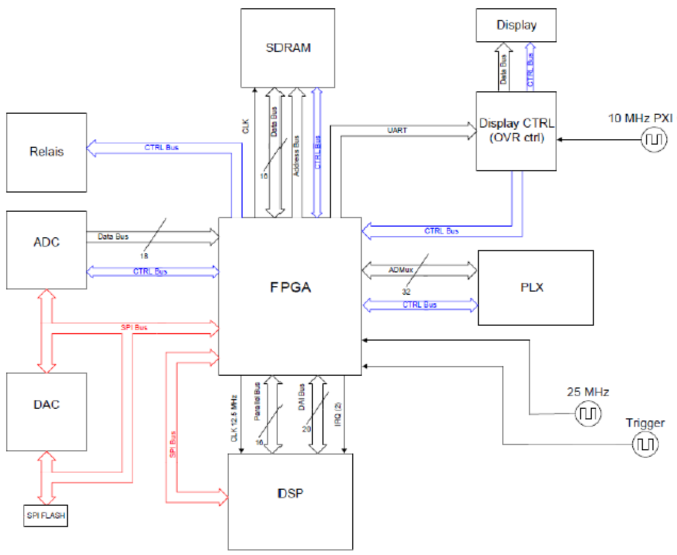


Fig. 1 Architecture of e-FDI.

### *2.1. Analogue front-end*

The analogue front end has to grant, like in the existing FDI, an accuracy of 1 ppm for at least 1 s, a 100 kHz bandwidth, and has been improved in terms of input matching characteristics and noise rejection. It consists of three main blocks: an input circuit, a programmable gain amplifier (PGA), and an instrumentation amplifier also implementing low-pass anti-alias filtering. The input circuitry is directly connected to the transducer and senses the differential input signal. It can be configured to exhibit either 1 MΩ or 50 Ω impedance and also offers 1/10 attenuation. The PGA is a fully-differential amplifier allowing for range selection by means of three gain values: 1, 10, and 100. The third block is an accurate amplifier with unitary gain, but optionally configurable with a gain of 10. It is characterized by a high common mode rejection and implements a Butterwort type low-pass filter, with configurable cut-off frequency for anti-alias purposes.

### *2.2. Digitizer and inherent calibration hardware*

The digitizer exploits an 18-bit successive approximation register (SAR) ADC, triggered up to 500 kSa/s, compatible with the 25 MHz time base for completing the whole SAR configuration t within the time interval delimited by two successive triggers.

The instrument can work as basic digitizer or digital integrator. It can be calibrated and its main errors, namely offset and gain error, compensated by means of processing. Differently from FDI, the e-FDI exploits supplemental hardware to implement a different self-calibration approach. This allows the digitizer to be verified in all the points of its characteristic, thus opening the way for more effective calibration and specific drift corrections algorithms. In particular, in place of the FDI solution using a high-quality resistive network supplied by an internal stable source, showing high undesired sensitivity to temperature, e-FDI deploys a couple of 20-bit DACs characterized by 1 ppm INL, 0.19 LSB long-term linearity and 0.05 ppm/°C. The reference voltage for the DACs is obtained by a ±10 V, 1.09 ppm/°C, 6 ppm/1000 h voltage reference. By supplying both the DACs with the ±10 V reference voltage, and letting them share the low point connection, a differential output is obtained.

### *2.3. Linear errors compensation and digital integration*

Apart numerical integration, the on-board DSP configures the two DACs during the calibration procedure, processes the digitized data to recognize linear errors, and performs error compensation.

The self-calibration procedure requires, for each selection of the front-end PGA gain, the following steps:

- dual DAC calibrator configuration and successive digitization of the known voltage level, until a representative set of input-output couples is collected;
- identification of gain and offset parameters of the straight line that best fits the data in the sense of minimum mean square error;
- estimation of the calibration data, i.e. parameters for offset and gain error compensation.

The DSP is responsible both of the DACs configuration via local SPI bus, and the linear errors identification, which is performed by applying linear regression algorithms. During the calibration procedure the input-output couples are collected and stored in the local SDRAM memory of the instrument, where they are overwritten by the calibration data after the completion of the processing. The calibration data are retrieved during the ordinary operation to correct the digitizer codes.

When connected to the transducer to digitize and integrate the input voltage, the DSP takes also care of integrating the digitized voltage values. At this aim, the 500 kSa/s data stream produced by the ADC is processed in real time. In particular, to avoid accuracy losses, the DSP firmware includes in the integrated data also the contribution of head and tail time intervals, which are limited: (i) the former, by the trigger event that starts the integration and the digitization of the first code within the interval, and (ii) the latter by the digitization of the last code acquired and the occurrence of the trigger event that stops the integration.

### *2.4. Control and data routing*

The control unit is implemented on an FPGA block, which at turning on of the instrument loads the bit-stream needed for the booth-strap from the local non-volatile memory. Among the main operations, the FPGA control unit manages the fine 25 MHz time base and provides the sampling clock to the ADC after frequency division, and measures in terms of basic counts the duration of the head and tail time intervals to be taken into account for digital integration. It also cares for interconnection and data exchange among on-board devices, since it is the hub of the serial peripheral interfaces (SPIs). On board SPIs are exploited to bridge connections between ADC, DACs, DSP, and the flash memory, which permanently saves service, bootstrap, and processing routines. Further data and control busses assure connections to (i) retrieve digitized data from ADC and process them by means of DSP, (ii) to download and fetch from SDRAM raw and processed data, and (iii) to let PLX controller of the peripheral interface to manage and transfer data to external devices, taking advantage of direct memory access operation mode.

### *2.5. Data transfer to external devices*

The e-FDI instrument uses a 32-bit PXI bus that is controlled by a PCI9056 hardware accelerator capable of functioning up to 66 MHz. With respect to the solution adopted by FDI, the new one, thanks to the direct memory access, allows great improvements in terms of operation frequency increased up to 40 MHz. In DMA master mode, data from the internal memory of the FPGA-based control unit are directly transferred to the external device, namely a PC.

## 3. METROLOGICAL CHARACTERIZATION

The metrological characterization of e-FDI involves both DC and AC tests; further tests are also needed to assess the instrument performance in terms of maximum data throughput. The metrological characterization is also designed to mainly investigate the performance required to e-FDI in the chief applications it is supposed to be employed: analysis of constant or slow-varying signals, such as ramps characterized by rising times ranging from tens of milliseconds to several seconds, as well as analysis of sinusoids characterized by frequencies ranging from some Hz up to a few hundreds of Hz. The static errors of the measurement chain, which includes all the blocks of the analogue front end, the 18-bit ADC, and the DSP based digital integrator, have been assessed by DC tests. In fact, since the instrument represents the output data as double-precision real numbers, standard approaches based on histogram tests, which are proposed to characterize ADCs, cannot be easy adapted to e-FDI. Thus, a calibration curve method is adopted for analysing the instrument output in correspondence of known inputs. The test points can be uniformly spaced along the whole range, or, alternatively, selected from the different octave intervals the whole range can be divided into. The latter approach should be preferred when it is likely that the non-linear behaviour of the instrument is mainly influenced by the SAR architecture of the ADC in the measurement chain. In both the cases, a linear regression method is applied to measured data to highlight offset, gain error, and local errors accounting for undesired non-linearity. Offset and gain error can be referred to as residual errors since the instrument runs a self-calibration procedure that aims at cancelling them; whilst non linearity errors are not contrasted by any compensation in the present version of e-FDI.

Tests with AC stimuli are aimed at highlighting both the harmonic distortion and inherent noise of the instrument. In these tests three parameters are considered: signal to non-harmonic ratio (SNHR), total harmonic distortion (THD), and signal to noise and distortion ratio (SINAD): SNHR informs about the inherent noise of the instrument, THD is instead a global parameter to express the overall distortion due to the instrument itself, and SINAD takes into account both the effects and is therefore to be considered if both noise and distortion are important. The first and second parameters can be conveniently measured in the frequency domain, provided data characterized by a data rate coherent to the frequency of the test signal are processed. For the third one, a sine-fit algorithm can be deployed to recognize the total effect of noise and distortion and compare its overall power to that of the signal.

## 4. EXPERIMENTAL RESULTS

### *4.1 Measurement set-up*

The experimental tests aimed at the metrological characterization of e-FDI are carried out by means of a measurement set-up that includes: an ADLINK rack hosting e-FDI equipped with a PXI interface, an external PC also equipped with a PXI interface, a DC calibrator Fluke 5442a, and a sine wave generator Stanford DS360.

For the metrological characterization, the standard regression algorithms and Fourier analysis have been carried out off-line.

### *4.2 DC tests results*

The residual offset and gain errors have been estimated considering both uniformly spaced and octave-distributed test points. Symmetrical positive and negative test points have been selected for a total even number $N$ of test points. Named $V_0$ the half-range of the instrument, the uniformly-spaced test points within the positive half-range have been chosen according to:

$$V_i^{(uniform)} = 2i\frac{V_0}{N}, \quad i = 1, \dots, \frac{N}{2} \qquad (1)$$

In the case of octave-distributed test points. instead a small set of $M$ uniformly spaced points has been considered within each octave interval. The attention has been limited to the larger $2P$ octave intervals and the test points within the positive half-range have been selected according to:

$$V_{i,j}^{(octave)} = \left(1 + \frac{j}{2M}\right)\frac{V_0}{2^i}, \quad i = 1, \dots, P; \; j = 1, \dots, M \qquad (2)$$

If $M$ is chosen equal to 1, a single test point coinciding with the middle point of each octave is selected.

The number of points considered in both the metrological tests has been the same, i.e. $N = 2PM$. It is also worth noting that the selection of the larger octave intervals, which are closer to the full-scale of the instrument, permits to avoid tests requiring very-low voltage inputs, for which the calibrator exhibits higher relative uncertainty.

Particular attention in DC tests has been paid to the values of the residual offset, which can originate drifts in long lasting tests. The e-FDI has shown typical residual offset values not superior to a few ppm units of the range.

### *4.3 AC tests results*

Two apparently contrasting requirements have to be taken into account when carrying out AC tests. In fact, the estimation of THD would benefit by sampling the input signal at a rate coherent with its frequency, since this allows to avoid scalloping-losses in the measurement of the fundamental and harmonics amplitude, which are required to quantify THD. But, coherent sampling is frequently responsible of clustering effects in the acquired data, which are instead to be avoided in order to homogeneously investigate the behaviour of the instrument upon the whole range. Fortunately, AC tests avoiding both clustering effects in the acquired data record, and at the same time scalloping-losses in spectral analysis, can be carried out. To this end, the minimum common multiple between the period of the test signal and the sample interval has to be equal to the duration of the acquisition interval. The same requirement can be also expressed by demanding that the greatest common divisor of both the frequency of the test signal and the sampling rate needs to be equal to the frequency resolution available in the spectral analysis. For instance, in the spectral analysis of a sinusoidal signal characterized by a frequency $f_0$ = 7.389 Hz and sampled at a rate $f_c$ = 1 kSa/s, both scalloping-losses and clustering effects are avoided if a frequency resolution equal to 1 mHz is assured. This is granted by collecting a data record containing $10^6$ samples, in which 7389 cycles of the input signal, each of them described with samples taken at different phases of the sinusoidal waveform, can be distinguished. From an operative point of view, if the sample rate $f_c$ and the memory size of the data record $R$ are given, the choice of the frequency $f_0$ of the test signal is restricted to a set of finite values. In particular, being $f_c = R\Delta f$, only the values $f_0 = S\Delta f$ in which $S$ is an integer sharing no common divisors with $R$, assure the requirements. In the aforementioned example $\Delta f = 1$ mHz, $R = 10^6 = 2^6 \cdot 5^6$, and $S = 7389\ 3^2 \cdot 821$ shared no common divisors with $R$. The use of prime number tables can be helpful at the test planning stage.

Test have been carried out by considering different combinations of sampling rates, frequency and amplitude of the input signal, and considering for the aforementioned parameters typical values that characterize the inputs that the instrument typically has to measure on field. Table 1 shows the results related to SNHR, THD and SINAD for input signals characterized by peak-to-peak amplitudes equal to 100%, 50% and 10% of e-FDI full-range, and for different selection of the front-end gain.

Table 1. Typical SNHR, THD, and SINAD of e-FDI for input frequency of 7.389 Hz and sampling rate 1 kSa/s.

| Front-end Gain | Fullscale [V] | Input Amplitude [% fullscale] | SNHR [dB] | THD [dB] | SINAD [dB] |
|---|---|---|---|---|---|
| 1 | 10.0 | 10 | **98.8** | **-95.3** | **97.8** |
| 1 | 10.0 | 50 | **99.5** | **-95.4** | **98.0** |
| 1 | 10.0 | 100 | **99.0** | **-96.3** | **98.1** |
| 10 | 1.0 | 10 | **97.8** | **-96.5** | **98.2** |
| 10 | 1.0 | 50 | **97.4** | **-97.7** | **98.3** |
| 10 | 1.0 | 100 | **97.2** | **-96.1** | **97.7** |

## 5. CONCLUSIONS

The results of the metrological characterization of e-FDI instrument have been shown and commented. The performance of the instrument is improved with respect to that of the previous version, namely FDI, in terms of DC accuracy, as well as noise and distortion rejection capabilities. The former improvement has been assured by the new self-calibration option included in the instrument, while the second has been granted by the modified front-end characterized by filtering functionality and high common mode noise rejection performance. A relevant improvement has been obtained also in the data transfer to external devices via peripheral interface by enabling direct memory access to the externals device itself.

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## REFERENCES


[1] P. Arpaia, A. Masi, and G. Spiezia. “Digital integrator for fast accurate measurement of magnetic flux by rotating coils”. In: Instrumentation and Measurement, IEEE Transactions on 56.2 (2007), pp. 216–220.

[2] P Arpaia, L Bottura, L Fiscarelli, and L Walckiers. “Performance of a fast digital integrator in on-field magnetic measurements for particle accelerators”. In: Review of Scientific Instruments 83.2 (2012), p. 024702.

[3] A. Ballarino, G. Montenero, and P. Arpaia. “Transformer-based Measurement of Critical Currents in Superconducting Cables: Tutorial 51”. In: IEEE Instrumentation and Measurement Magazine 8 (2014), p. 9.

[4] http://fdi2056.metrolab.com.

[5] P. Arpaia, P. Cimmino, and L. Fiscarelli. “Enhanced fast digital integrator for magnetic measurements”. In: 20th IMEKO TC4 International Symposium and 18th International Workshop on ADC Modelling and Testing, Benevento, Italy, September 15-17, ed. By IMEKO. 2014.

[6] L. Bottura, L. Larsson, S. Schloss, M. Schneider and N. Smirnov, "A fast sextupole probe for snapback measurement in the LHC dipoles," IEEE Transactions on Applied Superconducitvity, vol. 10(1):1435–1438, 2000.

[7] P. Arpaia, V. Inglese, G. Spiezia, S. Tiso, “Surface Response-Based Modeling of Digitizers: A Case Study on a Fast Digital Integrator at CERN”, IEEE Trans. on Instrum. and Meas,, Vol. 58, No. 6, June 2009.

[8] P. Arpaia, L.Bottura, A.Masi, G.Spiezia, “Performance Simulation of a Fast Digital Integrator for Magnetic Measurements at CERN”, Measurement, Vol. 41, No. 7, August 2008.

[9] P. Arpaia, L. Bottura, L. Fiscarelli, L. Walckiers, “Performance of a fast digital integrator in on-field magnetic measurements for particle accelerators”, AIP Review of Scientific Instruments, Vol. 83, No. 2, February, 2012, doi: 10.1063/1.3673000.

[10] P. Arpaia, L. Bottura, G. Montenero, S. Le Naour, “Performance improvement of a measurement station for superconducting cable test”, AIP Review of Scientific Instruments, Vol. 83, No. 9, September, 2012, doi: 10.1063/1.4752410.