DESIGN OF A VIRTUAL INSTRUMENT FOR ELECTRICAL POWER SYSTEMS WITH GENERATION OF DISTURBANCES

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Abstract − In this work, a Three-Phase Virtual Dummy Load able to generate six arbitrary distorted waveforms is described. The proposed system, is able to emulate a mono or three-phase system of symmetrical/asymmetrical voltages and a lot of different loads balanced or unbalanced and three types of disturbances. The proposed system is the testbed for a PQ energy meter prototype and is also useful to validate new algorithms for PQ events identification implementable in embedded systems.

Keywords: Power quality; Power system measurements; Signal synthesis; Data acquisition; Virtual instruments

1. INTRODUCTION

Today accurate measurement has become of great interest in Smart Grids and renewable energy field [1]-[3] where sudden changes in production and consumption threaten the stability of the network and security. Power Quality (PQ) measurements are fundamental for electric Power Systems (PSs) management since they ensure the quality of energy delivered to various kind of users.

An important issue is the metrological characterization of instruments adopted for PQ measurements also considering possible combinations of different phenomena at different severity levels [4], [5]. In such scenario, a useful solution to test new devices and algorithms in a lot of different operating conditions consists in using AC Electronic Load.

Another typical solution is to generate independent waveforms for voltage and current simulating a Dummy Load [6], [7]. The simulated PQ events can be used to test and to calibrate instruments for PQ monitoring or to evaluate PQ analysis algorithms.

In this work, the authors present a Three-Phase Virtual Dummy Load (3Φ-VDL) implemented using a National Instruments PXI-based (PCI eXtensions for Instrumentation) synthetic instrument to generate six arbitrary distorted waveforms (Fig. 1). All parameters of the synthetized signals are settable by a LabVIEW® user interface described in Section 2. The proposed 3Φ-VDL will be used as a testing tool in a project framework, which comprises the design of a prototype of a PQ energy meter. In its stable release, it will replace the actually used electromechanical Dummy Load [8] and will be used to validate a new algorithm developed by the authors for estimating the spectral content of frequency and amplitude modulated waveforms [9] [10].

In the following, Section 2 presents the technique for synthetizing signals and disturbances using LabVIEW code and the features of developed simulation software; Section 3 describes the hardware used for generation and its specifications while Section 4 describes a set of generated signals for verifying the proposed system and the future objectives are drawn.

Fig. 1.   3Φ-VDL block scheme.

2. SOFTWARE DESCRIPTION

There are many PS simulation tools available in literature [11] but fundamentally, there are two kinds of approaches: the modelling of PS components (distribution line, transformer, induction motors, capacitor banks, etc.) and the waveform modelling by means of parametric equations.

The former approach is oriented mainly to PS design or management and is deployed using circuit simulation software such as ETAP, PSCAD or Simulink to cite only a few examples [11], [12]. The latter approach is more general and useful for testing or calibration of the PQ instruments. In [13] is designed a simple virtual signal generator, for educational purposes, using LabVIEW and a sound card, while in [14] LabVIEW is used as a frontend to display waveforms and manage parameters of PQ disturbances simulated with a MATLAB script code. Other solutions are available in open-source platforms such as Python [9].

2.1. User interface

The 3Φ-VDL is designed in LabVIEW® using both built-in blocks and custom-built subVIs: the formers are used to

generate six independent multi-tones waveforms, while the latters permit to parameterize a set of possible distortions (dips, swells, interharmonics and frequency fluctuation). If needed the synthetized waveforms is scaled in the range -10÷10 V by a constant k_v (or k_i) and then sent to a multifunction DAQ board in order to generate the output signals.
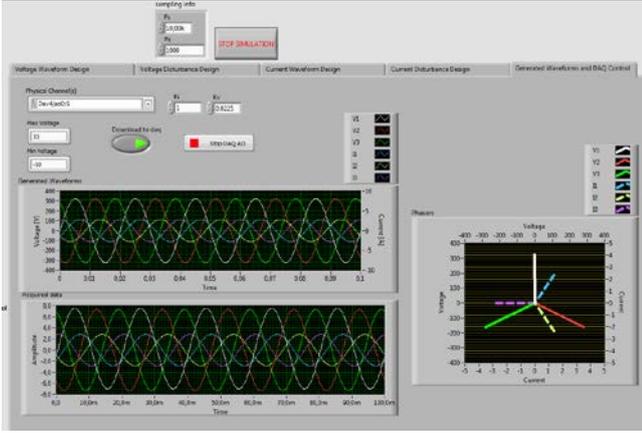

Fig. 2.   3Φ Virtual Dummy Load front panel

The front panel (Fig. 2) consists of five tabs: two to configure the voltage waveforms (i.e. Voltage Waveforms design and Voltage Disturbances design), two to design the line currents while the last tab contains the waveform Graphs to display the designed waveforms and the phasors of main components and some controls to configure the DAQ board and to simulate the presence of voltage and current transducers (k_v and k_i).

3Φ-VDL Structure

The design of user interface follows the paradigm of modular and hierarchical programming in order to permit future development and easy integration of new features.

The main Virtual Instrument (VI) - *Three Phase Virtual Dummy Load.vi* - contains two identical subVIs (Fig. 3), one representing line voltages and the other representing line currents, each of them has in input three *3xN* matrices (L1, L2 an L3); *N* is an arbitrary harmonic order. Each column of the matrix contains frequency, RMS value and phase of the relevant harmonic. Thus, the three voltage (current) waveforms are composed of a sum of sinusoids.
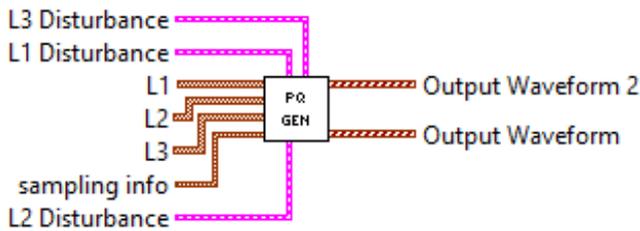
Fig. 3.   VirtualPQGenerator.vi

The described VI builds a 3xM matrix where M in the number of samples defined by the user with the cluster Sampling Info which contains also the sampling frequency value.

The fundamental component of the L1 output voltage can be represented as:

$$v_1(t) = \sqrt{2}V_{1RMS}\sin(2\pi f g(t) + \varphi) \qquad (1)$$

V_{1RMS} is the rms value of L1 voltage, *f* is the fundamental frequency and *φ* is the initial phase.

The waveforms are then passed to a frequency modulator block in which a simple modulation function is implemented.
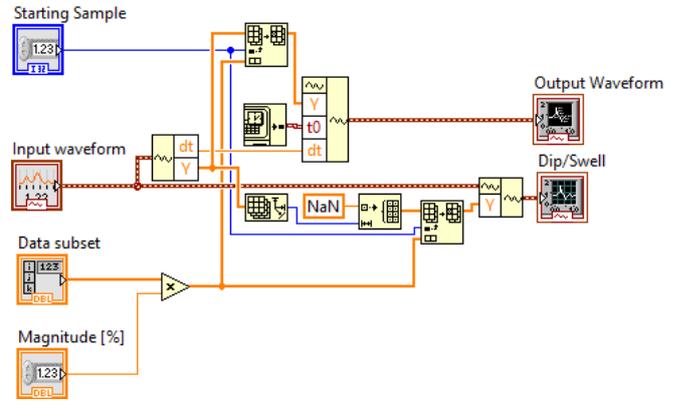
Fig. 4.   Block diagram of the dip/swell generator

The actual implemented frequency modulation g(t) is:

$$g(t) = t + A\sin(2\pi Bt) \qquad (2)$$

where *A* and *B* are user-defined parameters. Obviously, *g(t)* can be easily replaced by any other frequency modulation function.

After the frequency modulator block, the *"Extract Portion of Signal"* express VI allows a number of samples to be extracted from the waveforms. In Fig. 5 it is possible to view the block diagram of the described procedure and have a more clear representation of the data flow.

3. HARDWARE DESCRIPTION

In this work, the developed 3Φ-VDL hardware architecture is based on a modular PXI system. All used modules are mounted into a PXI Express chassis by National Instruments (NI) model PXIe-1065 [15]. A laptop computer controls the chassis by means of a NI ExpressCard-to-MXI bridge based on an ExpressCard-8360 connected and a NI PXIe-8360 module. (Fig. 1 and Fig. 6).
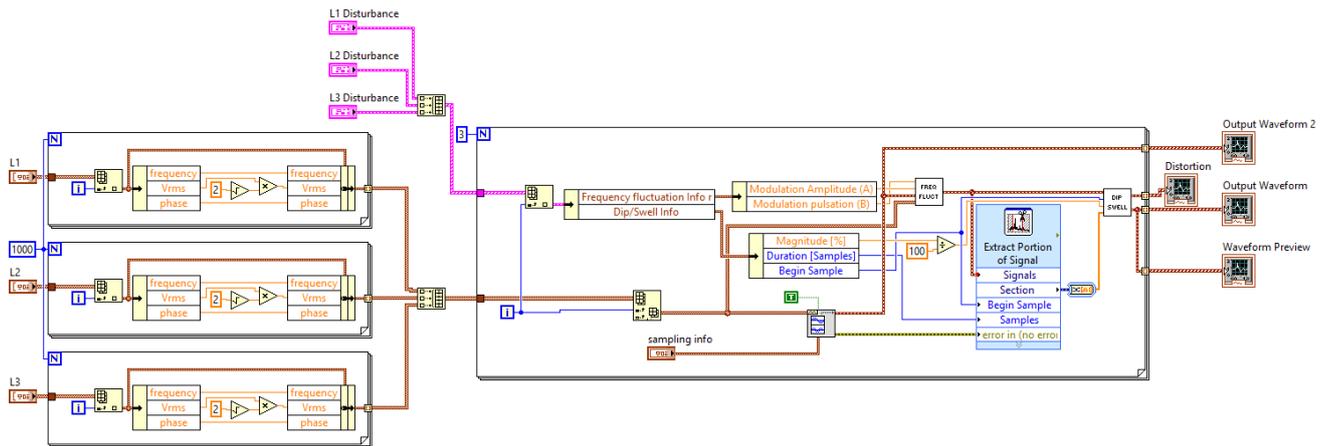
Fig. 5.   Block diagram of the *VirtualPQGenerator.vi*

The source of the real generated signals is a Multifunction DAQ device model NI PXI-6713, an high speed Analog Output module with eight 12-bits channels, with a maximum refresh rate of 1 MS/s per channel [16]. The signals are dispatched by means of a NI BNC-2110 Connector Block.

In order to monitor the real generated waveforms a NI PXI-6052E module is used. This module can digitize and stream data to a PC at rates up to 333 kS/s [17].
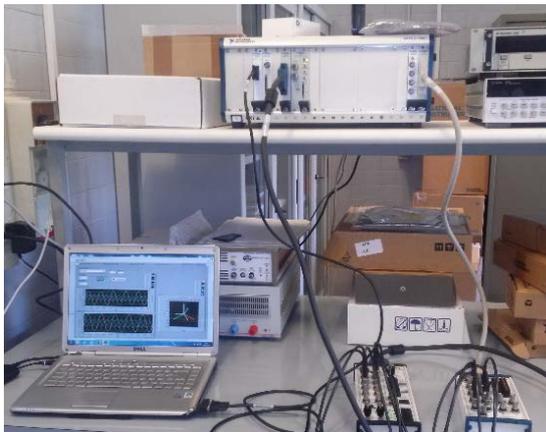

Fig. 6.   3Φ-VDL System

The proposed architecture is only an example of 3Φ-VDL possible hardware implementation; other solutions may involve more accurate or cheaper DAQ devices. For example in [18] the authors used a Dynamic Signal Analyzer Series board model NI PXI-4461 to characterize the acquisition channels of a developed PQ energy meter. The user interface is hardware independent thus it is possible to reconfigure some blocks to fit the application to the available hardware. For this reasons the proposed 3Φ-VDL represents a valid and flexible solution for both research and educational purposes.

4. EXPERIMENTAL RESULTS AND FUTURE WORK

With the 3Φ-VDL it is possible to generate three-phase systems with symmetric/asymmetric voltages and to simulate several different types of balanced or unbalanced loads (ohmic, ohmic-inductive, ohmic-capacitive, inductive, and capacitive) and basically three types of disturbances:

1. Dip/swell
2. Harmonics/interharmonics
3. Frequency fluctuations

It is also possible to mix these disturbances to create an arbitrary combination of them.

For example in Fig. 2 the front panel shows the simplest case of a three-phase low-voltage system (230 Volts rms) and a 2 Amps rms balanced load (ohmic-inductive). The waveform graph at the bottom displays the waveforms acquired for debugging purposes to demonstrate the coherence between the designed waveforms and the acquired ones.
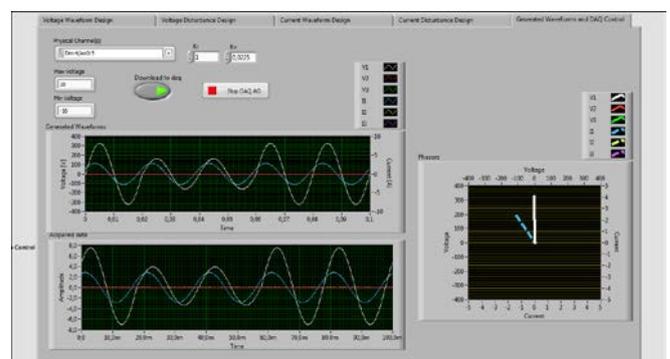
Fig. 7.   Simulation of a single phase PS made by an ohmic-capacitive load and a voltage dip (50% reduction factor).

Fig. 7 reports the simulation of single-phase power system made by an ohmic-capacitive load where a voltage dip with a reduction factor of 50% and a duration of 0.4 ms is simulated.

Fig. 8 shows another example: a three-phase power system with a third-order harmonic component where the voltage V1 is affected by a dip (with the same characteristics of the previous case) while, at the same time, the voltage V2 is swelled (120% of nominal value). Finally, Fig. 9, presents a frequency fluctuation acting only on phase 1; the waveform is obtained considering the expression (2) where A = 0.009 and B = 3.

The previous examples should give and idea of the capabilities of this tool in combining a set of disturbances.

The 3Φ-VDL development is still in progress, new features will be implemented soon (flicker, notch, transient, etc.). Actually the system can be connected only after the analog front end (at the ADC level) of any PQ devices since the maximum voltage available to the BNC-2110 terminals is ±10 V.

For the final implementation the generated signals must be conveniently amplified and this will require one or more High-Voltage Power Amplifier (like the PZD700A by Trek [19]) for voltage signals, and a 4-quadrants power supply (like TOE 7621-20 by Toellner [20]) for the current signals. With the cited amplifiers it would be possible to emulate a real PS where the voltage output range will be up to 700 V (peak) with a bandwidth greater than 150 kHz, while the output current range will be 16 A with a bandwidth of 100 kHz.
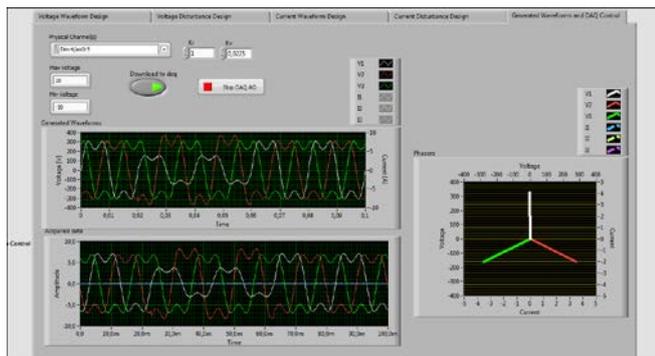
Fig. 8. Simulation of a three-phase voltage system with a third-order harmonic component where the voltage V1 is affected by a dip while, at the same time, the voltage V2 is swelled
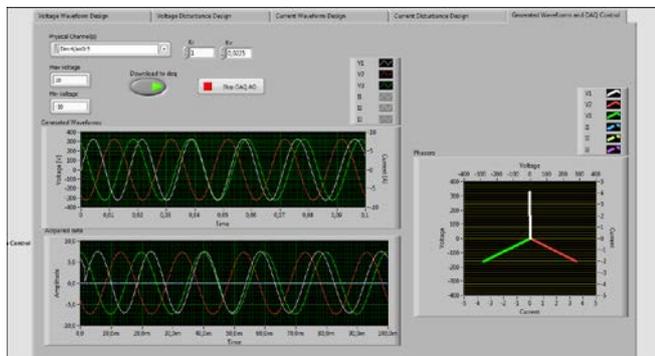

Fig. 9. Simulation of a frequency fluctuation acting only on voltage V1.

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