XXI IMEKO World Congress "Measurement in Research and Industry"
August 30 - September 4, 2015, Prague, Czech Republic

PARTIAL DISCHARGE DIAGNOSTIC SYSTEM FOR NON-DESTRUCTIVE TESTING OF HIGH-VOLTAGE MACHINES

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Abstract **-** This paper deals with the complex design of the partial discharge system for high-voltage machines diagnostics. The result of the work is complete measurement system, which fulfils specified functionality. Implementation relies on the FPGA with the advantage of system-on-the-chip technology. This solution enables flexible and powerful signal processing. Measurement principles and methods together with the test results are also mentioned.

Keywords: partial discharge, diagnostics, FPGA, system-on-the-chip,

1. INTRODUCTION

Upcoming trends in reliability increasement and cost lowering of the high power machinery maintenance are the main reasons for research and develop activities in this field. It is able to prevent large failures of the mentioned appliances by correct and planned diagnostic steps. These steps could extend the lifetime of the particular device and avoid cost ineffective replacements of the parts.

There are several diagnostic methods which are used for destructive or non-destructive inspection of the high-voltage power rotary and non-rotary machines (power generator, transforms etc.). The well known non-destructive methods acc. to [1] are partial discharge measurement and dissipation factor and capacitance measurement.

2. PARTIAL DISCHARGE

Partial discharge (hereinafter as PD) is localized electrical discharge, which partially shortcircuits the insulation between conductors. The measurement system works with the incidence of the *PD impulse* acc. to [2]. This current impulse is result of the PD inside the device-under-test (hereinafter DUT). Time duration of this event is typically significantly shorter than $10\,\mu s$.

2.1. Impulse shape and its measurement

The measured value of partial discharge impulse is charge Q. Charge is defined as follows:

$$Q = \int I\,dt \tag{1}$$

To satisfy this equation the digitalized signal of current should be discretely integrated and the area under the curve should be estimated acc. to [3]. Basic impulse shape of the signal is described in [4]. This value directly correspond with the partial discharge impulse. The discrete summation is shown below:

$$Q = \sum_{k=i_{start}}^{i_{end}} I[k] \cdot \frac{1}{f_s} \tag{2}$$

where i_{start} and i_{end} are indices of the start and the end of the impulse, the $I[k]$ then the discrete value of the current at particular moment and f_s is the sampling frequency used in the digitizer. Anyway, there is no specific instructions in the [2] how to determine and handle signal analysis especially with modern digital instruments. This task is typically hidden inside proprietary algorithms of modern devices.

2.2. Measurement chain

Basic measurement chain is shown in Fig. 1. This fundamental connection relies on the AC testing voltage in range up to nominal voltage of the particular machine. This source excites the DUT and the signal leads to the PD Meter via the coupling capacitance.

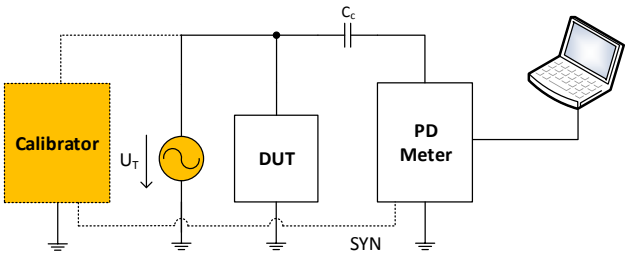

Fig. 1. Basic measurement chain

Inside sub-parts of the PD meter are able to split up the input signal to the testing voltage signal and filter out the PD events current signal. This is done by the coupling device which is the front-end of the PD meter. Functional diagram of the coupling device is shown in Fig. 2.

3. PD METER DESIGN

The whole diagnostic system consists of the PD meter and calibrator. The design and features of the FPGA based PD meter will be described in this part of the paper. This device consists of three sub-parts. As it was mentioned

earlier the first front-end part is the coupling device. Sampling of signals, controlling and communication are done by the digitizer board. Power source and supervisory circuits of the battery cells are integrated at the accupack board.

3.1. Coupling device

Coupling device implements two measuring paths. First path is for the PD events and implements band-pass filter with working range from $30\,kHz$ to $2\,MHz$ which fulfils requirements in [2]. One of the basic function is to adapt the input voltage amplitude to the measuring range of the digitizer. This is done mainly for the testing voltage measuring purposes. The input voltage U_t is divided by the capacitance divider which is formed by the coupling capacitance and internal capacitance of the coupling device. Adapted signal continues to the second signal path which consists of the low pass filter. More details about the measuring path and gain control is shown in Fig. 3.

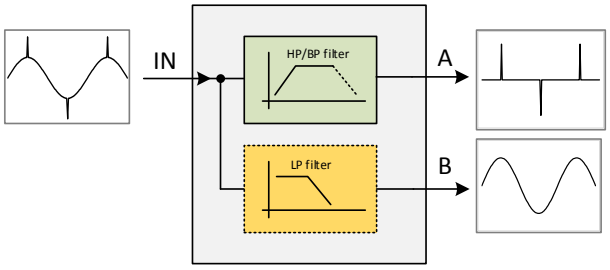

Fig. 2. Functions of the coupling device

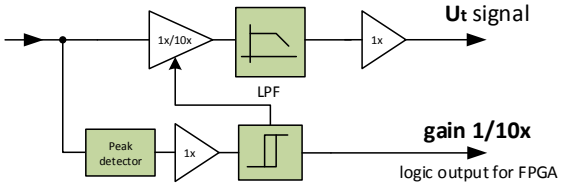

Fig. 3. Measuring path for testing voltage

3.2. Digitizer board

The complete control, digitalization and signal processing is done at the digitizer board. A lot of parallel tasks are taking into account in such an application. Sampling and analysing of PD events and the testing voltage signal simultaneously are the main task. Block diagram of the analog front-end parts is shown in Fig. 4. The sampling frequency of the analog-to-digital converters at inputs is $f_s = 50\,MSPs$. Each channel has its own programmable gain amplifier with gain range from $-11.5\,dB$ up to $20.0\,dB$. The core component is the FPGA Altera Cyclone IV GX which implements all logic

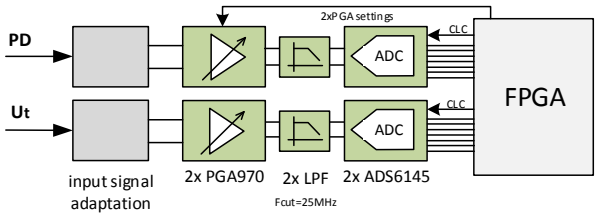

Fig. 4. Analog to digital front-end of digitizer board

inside the PD meter. Memory space for samples and run-time dependencies consists of two separate SDRAM blocks each 64 MB. The separate implementation ensures true parallel operation with two memory controllers designed inside FPGA. The uplink connection is one of the most important parts. This channel is fully galvanically isolated. To avoid proprietary protocols the PD meter communication works with TCP/IP protocol and acts like a network device in LAN networks. The FPGA Cyclone GX allows to use Serial Gigabit Media Independent Interface (SGMII). Network interface are flexible because of the SFP module compatibility. With variety of SFP modules the user can use fiber or wire connection at several speed links up to $1\,Gbps$.

All tasks of the FPGA are controlled from SoC system with built-in software processor NIOS II F. The runtime code for measuring, controlling and communication tasks are managed by RTOS operating system, which is loaded on the processor.

Last sub-part of the digitizer is the power source. Four Li-Ion cells each capacity $3400\,mAh$ have been used in 2s2p connection to fulfil the voltage and battery lifetime requirements of whole diagnostic system.

4. CALIBRATION

An integral part of the PD measurement systems are the calibration process. This process is used before each diagnostic measurement at the particular location. The typical calibration connection to the DUT is shown in dashed line in Fig.1.

The calibrator produces required amount of the charge on its output, which is used for the calibration of the whole measuring chain including cables, connection. Operator will set-up the PD Meter to obtain correct measured values during this process. The PD meter is synchronized via external SYN pulse from the calibrator instead of the AC test voltage zero-cross sensing.

4.1. Fully-digital calibrator

The basic principal of the calibrator is producing required charge given by:

$$Q = CU \tag{3}$$

where U is square-wave excitation signal connected in series capacitor with capacitance C like in [5]. This

paper describes design of fully-digital calibrator which adds several features which are not able to implement with basic approach. In this implementation user can set the charge amount in several steps. Currently supported base values are $100\,pC$, $1\,nC$, $10\,nC$ and their multiples 2x, 5x. The highest possible charge is $100\,nC$. Output stage is shown in Fig. 5.

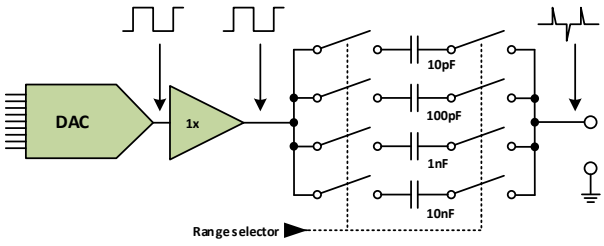

Fig. 5. Calibrator output stage

In contrast with other calibrators, this device supports more than two PD events in one period. All settings are accessible via built-in display. User can control the calibrator directly via control application for the PD meter through RS 485 connection link between these devices.

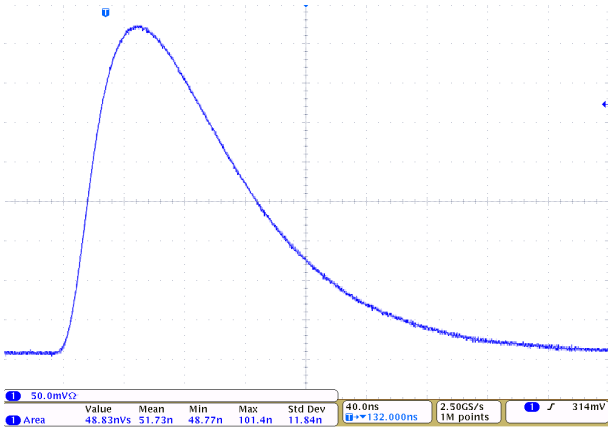

Fig. 6. $1\,nC$ charge sensed via 50 ohm resistance

This device is battery operated and is equipped by user's controls, so it can operate separately without the PD meter. In addition, this device and all charge ranges could be directly recalibrated using password locked menu on the control display.

Calibrator parameters and features have been tested with digital oscilloscope and several modes have been verified. Fig. 6 shows output charge of $1\,nC$, which has been measured with purely resistive load of $50\,ohm$. Parallel load combination of capacitance and resistance has been also tested. The result is in Fig. 7. The waveform consists of several reflections and imperfections so more complex digital signal process should take place.

There are several other major factors which can lead to the signal deformation. The majority of connections should be done by coaxial cables. Single-ended terminal wires

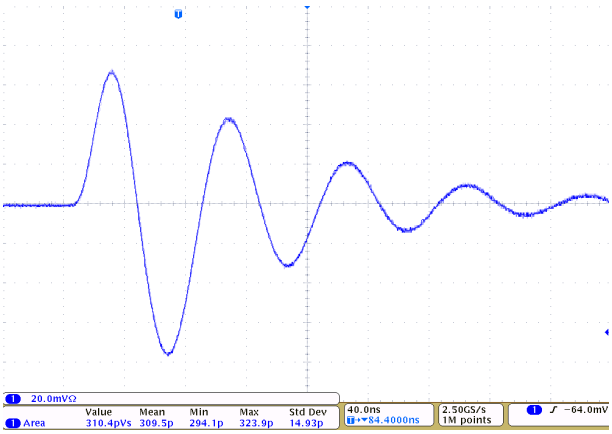

Fig. 7. $1\,nC$ charge sensed via $50\,ohm$ resistance in parallel with $1\,\mu F$ capacitance

should be as short as possible. Long cables will also add capacitance to the measuring circuit.

5. PD EVENT ANALYSIS

To prepare data for PD event analysis some basic signal processing steps must take place. The typical measuring environment cause several issues like higher noise level presence in the PD signal. These basic algorithms are directly placed in FPGA using VHDL code blocks. First step is an offset correction. The offset level is estimated as the mean value of the PD signal during each period. This step is necessary for the PD events localization and correct area integration. The noise level can be selected by user or estimated automatically. Second step is simple noise cancellation. All samples which satisfy the condition

$$|I| < noise \tag{4}$$

are set to zero. Third step is the area integration, which belongs to the PD events. The runtime process in VHDL analyses the samples after offset and noise correction and calculating difference between each two samples. If the samples satisfy this condition

$$|I[k+1] - I[k]| > diff_{set} \tag{5}$$

the summing process of the impulse samples begins. The $diff_{set}$ is a parameter set by operator through PC application. The summing process then continue until the samples are positive if the calculated difference was positive or negative if the calculated difference was negative. Thanks to this approach, there is a possibility to detect both polarities of the PD events. Afterwards the deadtime postpones any other PD event localization. This mechanism eliminate sensing the false PD events. This algorithm is illustrated in Fig.9. False PD events are could be caused by reflections which are result of impedance mismatched connections. User can choose from two possible data view modes. Both options are available via PC control application.

6. OPERATING MODES

6.1. Full-expert

First type is a **full-expert mode**, where all datasets are directly transferred to computer for post analysis. Basic visualization is shown in Fig. 8. This mode is useful for the first few measurements at any new location for important parameter estimation like offset and noise.

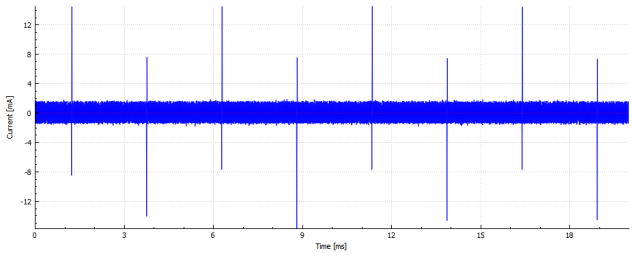

Fig. 8. Full-expert visualization of the 20 ms period

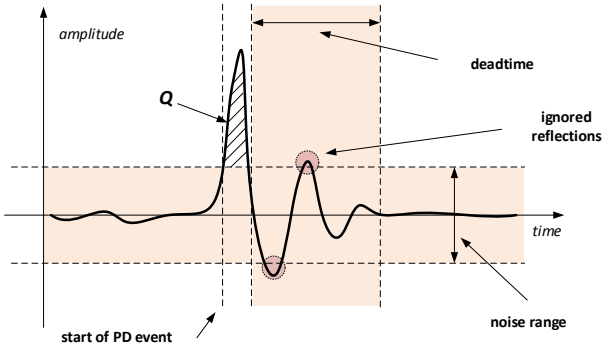

Fig. 9. PD event localization

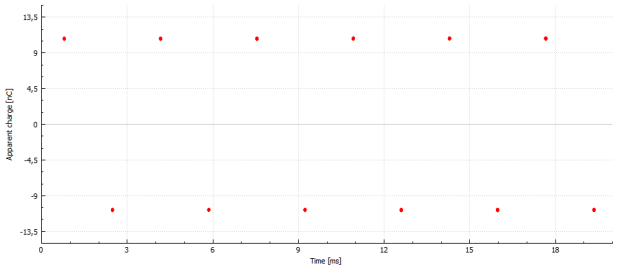

Fig. 10. Phase-resolved PD pattern (12 PD events from calibrator)

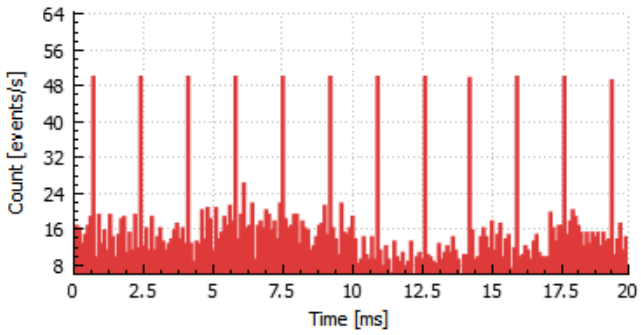

Fig. 11. Histogram of PD events (12 PD events from calibrator)

In this mode the third step of signal processing inside the FPGA does not take into account. The integration could be done in the same way but on the already sampled waveform.

6.2. Real-time or on-the-fly mode

Second mode is available for **real-time** or **on-the-fly** measurement. The PC application visualization of the phase-resolved PD pattern like in [6] is shown in Fig. 10. This mode uses all three steps of signal processing and PD charge size estimation inside FPGA core. Operator obtains only relevant data about PD events and all necessary statistics are calculated on the fly. User can list out all PD events which have been determined by the FPGA logic.

6.3. Useful tools

Operator can also use PD event histogram as a helpful tool to check if the high power machinery discharges have some typical periodicity. For instance in Fig. 11 is obvious that PD events are in each $1.66\,ms$ step. This corresponds with 12 PD events in one period. Other displayed events are not periodically represented in each period. Setting up noise level too low causes such a result, because some noise will pass to the signal processing chain. If some parts of the signal is very noise or consists false events, user can filter out this time interval with window filter tool.

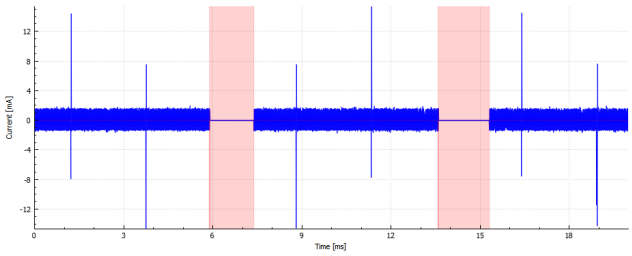

Fig. 12. Window filter tool (two zones defined)

Several parameters are calculated immediately during the real-time mode. The main values are discharge average current I, discharge power P, discharge count N and average discharge $Qavg$.

7. VERIFICATION

At the first step the designed calibrator has been calibrated by means of reference resistance normal and digital oscilloscope. The linearity of the PD meter has been tested with the direct connection of its input to the calibrator output port. The measured results has shown that the error of non-linearity of the charge estimation is below 3 %. This fact fulfils the requirements resulting from [2]. The Fig. 13 shows results of the real PD measurement. The measured DUT was high-voltage capacitor with similar capacitance as high-voltage transformer winding. Excitation voltage was $6\,kVrms$, while the largest PD events had charge near $1nC$ and their count in one period was about 2000 to 3000 events.

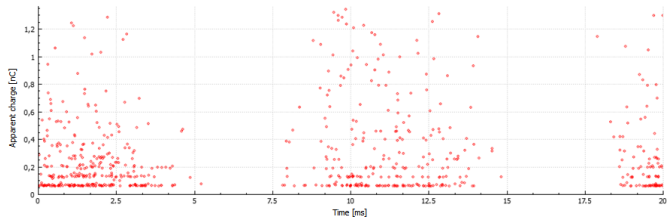

Fig. 13. PD events measured on real DUT @ $6\,kVrms$

8. CONCLUSION

This paper dealt with a design of a fully-digital system for partial discharge measurement in the field of high-voltage machines diagnostics.

Fig. 14. Two complete diagnostic sets
(PD meter at the bottom, calibrator at the top)

The results of the work are shown in the Fig. 14. Several measurements has been done to verify functionality of whole diagnostic set. The passband of the input coupling device has been verified to satisfy the recommendation according to [2]. The PD meter has direct Ethernet LAN connection with possibility to interconnect more than one PD meter to achieve poly-phase measurements. PC application offers several visualization options and complete control of system. Summary of both devices parameters are shown in Tab. 1 respectively Tab. 2. Calibrator device has been designed in order to directly cooperate with the PD meter or to work independently. The future work will focus on the performance improvement of the PD meter. One of the possible areas of discharge measurement is cable and wiring testing during its manufacture process. Typical charge range in these applications is less than $10\,pC$. To achieve this accuracy for such a low values the current sampling frequency should be increased at least five to ten times. Also the up-link communication speed could be improved to achieve faster data transfers from the instrument to the computer.

Table 1. Basic parameters of PD meter.

Parameter	Value
Charge measuring range	100 pC - 100 nC
Maximum input voltage	100 kV @ $Cc = 1\,nF$
Internal capacitance	$11\,\mu F$
Sampling frequency	50 MSPs
Memory size	128 MB
Battery life	8 h +
Battery parameters	8.4 V 6.8 Ah
Uplink interface	SFP module (LAN)
Calibrator interface	RS 485
Dimensions	220 mm x 125 mm x 52 mm

Table 2. Basic parameters of charge calibrator.

Parameter	Value
Output charge	100 pC - 100 nC
Pulse count	2, 4, 6, 8, 10, 12
Period duration	20 ms
Synchronization	2x TTL output
Battery life	12 h +
Battery parameters	$\pm$8.4 V 3.4Ah
PD meter interface	RS 485
Dimensions	120 mm x 103 mm x 53 mm

ACKNOWLEDGEMENTS

This work has been financial supported by Technology Agency of the Czech Republic in the framework of project No. TA02010311 "Intelligent measuring diagnostic system for estimation of operational state of high voltage electrical rotary and non-rotary machines".

REFERENCES

[1] Schwarz, R.; Muhr, M., "Diagnostic methods for transformers", *Condition Monitoring and Diagnosis, 2008. CMD 2008. International Conference on*, pp.974,977, 21-24 April 2008.

[2] IEC 60270:2000, *High-voltage test techniques - Partial discharge measurements*, Dec. 2001.

[3] Fauser E. Brosche T. Hiller W, "Novel Characterization of PD Signals by real-time measurement", *IEEE Transactions on Dielectrics and Electrical Insulation*, Feb. 1999.

[4] Bartnikas, R., "Partial discharges. Their mechanism, detection and measurement" *Dielectrics and Electrical Insulation, IEEE Transactions on*, vol.9, no.5, pp.763,808, Oct 2002 doi: 10.1109/TDEI.2002.1038663

[5] Chiampi, M.; Crotti, G.; Yue Hu; Sardi, A, "Development and Application of a Programmable Partial Discharge Calibrator", *Instrumentation and Measurement, IEEE Transactions on*, vol.58, no.4, pp. 768,774, April 2009.

[6] Gulski, E., "Digital analysis of partial discharges," *Dielectrics and Electrical Insulation, IEEE Transactions on*, vol.2, no.5, pp.822,837, Oct 1995 doi: 10.1109/94.469977