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IMPROVEMENT OF THE TIME-INTERVAL MEASUREMENT SYSTEM PARAMETERS BY MULTIPLICATION THE NUMBER OF ITS COMPONENTS

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Abstract **-** The paper contains description of TI (Time-Interval) measurement system implemented in FPGA (Field-Programmable-Gate-Array) structure whose such parameters as measuring uncertainty and maximal intensity of registered TSs (Time-Stamp) have been improved by the multiplication the number of its components. In this research the resolution has been increased by multiple TDL (Tapped-Delay-Line) use and the maximal intensity has been increased by hardware parallel processing implementation.

Keywords: FPGA, time-interval, histogram, time-stamp, tapped-delay-line

1. INTRODUCTION

TIMSs (Time-Interval-Measuring-System) can have many applications in science engineering and industry [1, 2, 3]. They can also be realised in many ways [2, 4, 5, 6]. TIMSs can be used directly or indirectly to measure other quantities by converting them temporarily to TIs [2]. Depending on use domain and implementation technology TIMS can vary in properties and can differ in cost [1, 2]. The most important parameters of TIMSs are measurement-resolution, measurement-range and maximal intensity of registered TSs [3].

The measurement-resolution of TIMS can be improved by applying the Vernier method [7], the interpolation and the multiple-stage interpolation [5], the time-stretching or multiple-measurement [2]. The first two mentioned methods utilize TDLs and the TIMS resolution is determined by TDL segment delay-value [8, 9, 1]. The TDL segment delay-value can be decreased either by using MTDL (Multiple TDL) or by changing implementation technology to the finer one [5]. The time-stretching decreases the maximal intensity of registered TSs but can be applied with connection with any other method. Multiple-measurement can also be connected with any other method and can be realized either parallelly or sequentionally [2].

The measurement-range can be extended by standard-clock period counter implementation, but is limited by long-term standard-clock stability [1, 2]. The maximal intensity of registered TSs usually can be increased by parallelization of critical TIMM (Time-Interval-Measuring-Module) blocks or by changing implementation technology to the faster one [1]. Currently the FPGA and the ASIC (Application-Specific-Integrated-Circuit) are two technologies that play an important role for TIMM implementation [10, 11, 12, 13]. Both these technologies allows implementing regularly-placed elements of equal delay that are necessary to construct TDLs [3, 2].

When multiple-measurement is used the correlation of measurements plays an important role. In case when measurements are not correlated the average-value standard-deviation of n measurements is decreased $\sqrt{n}$ times [3, 14].

The code-converter and the acquisition hardware are the main bottlenecks of TIMMs [1]. During the conversion process no other pulses can be registered till conversion has been finished and converted data has been written. To increase the maximal intensity of registered TSs n times one can increase the number of code-converters and acquisition-units just n times. After such modification every hit can be processed by another hardware simultaneously. Then the only limitation of the maximal-intensity of registered TSs is TDL-register propagation-time, that usually is much less than code-conversion time.

2. PRINCIPLES OF TIME-INTERVAL MEASUREMENT

TI between two consecutive events can be calculated as the difference between TSs generated by these events. TS values are specified relatively to standard-clock signal CLOCK (Fig. 1). Physically these events are represented by rising-edges of the signal PULSES. To obtain TS value for rising-edge of i-th pulse the number N_i of standard-clock periods that appeared since TDC initialization and time-offset P_i between the rising-edge of the signal PULSES and directly preceding it the rising-edge of the signal CLOCK must be obtained.

The TIMM consists of TDL that is responsible for measure-resolution increase and the pair counter-register (CNT, REG) that is responsible for the measuring range extension (Fig. 2).

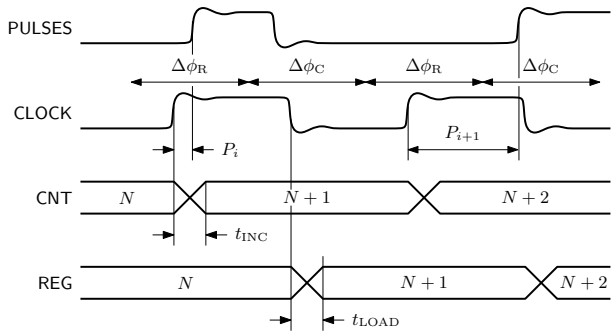

Fig. 1. Time-interval measurement idea.

The time-offset P_i is determined by TDL with precision that equals to TDL segment delay-value (Fig. 1). To obtain the number of standard-clock periods N_i the pair of binary counter CNT that increments every standard-clock rising-edge and register REG that loads the counter-state every standard-clock falling-edge must be implemented. The presence of this mutually-complementing pair is necessary because events occur asynchronously to standard-clock. In case when the PULSE rising-edge appears in the counter incrementation surrounding t_{INC} the information about the standard-clock periods number should be read from the register. Analogically, when the PULSE rising-edge appears during the register is being loaded (t_{LOAD}) the information about the standard-clock periods number should be read from the counter.

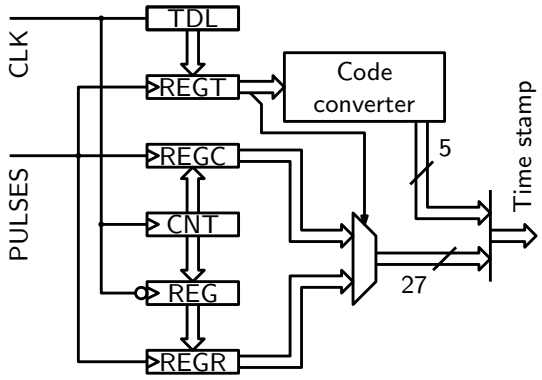

Fig. 2. Time-interval measuring module.

Every rising edge of the signal PULSES registers the state of TDL in register REGT and the state of CNT-REG pair in registers REGC and REGR (Fig. 2). Every rising edge of CLK increments the standard-clock period counter and starts the new phase in TDL. Whereas every falling edge o CLK registers the CNT state in register REG.

The TDL provides information in some kind of thermometric-code about the standard-clock (CLK) phase for the PULSES rising edge appearance. Then this information is converted to natural-binary-code to limit the number of occupied bits. Let us suppose that the TDL posses 32 segments (taps). Then the information can be compressed to 5 bits, that form the least significant bits of the result (time-stamp).

The most significant bits of the result are obtained either from counter CNT (strictly speaking REGC) or from register REG (REGR) depending on the value registered in TDL register (REGT), so depending on standard-clock (CLK) phase. Generally standard-clock CLK and signal PULSES are asynchronous. This means that rising edges of CLK (CNT incrementation) and PULSES (CNT registration in REGC) may appear very closely in time. To avoid counter-mistakes in such cases the information about standard-clock period-number is read from REG (REGR) that was written a half a standard-clock period before. Analogically when rising edge of signal PULSES appears close in time to falling edge of CLK, the information about standard-clock period-number is read from CNT (REGC).

TS (Fig. 2) refers the PULSES rising-edge appearance to standard-clock CLK. To obtain TI one needs to perform the subtraction of two following TSs.

3. MEASUREMENT UNCERTAINTY IMPROVEMENT

To minimise measurement uncertainty one can increase the number of measurements, but this solution also increases the time of measure. This approach is only available for periodic processes. Another solution is to increase the number of meters. Then the measure time does not increase while the the number of measurements increases. Very often not the whole measuring module have to be duplicated, but only its selected parts.

To increase the number of measured TIs one has only to increase the number of TDLs and code-converters (Fig. 4). All measurements can be treated as uncorrelated because of TDLs non-linearities. By the use of 16 TDLs the uncertainty of the average value decreases 4 times.

The module has been implemented into Xilinx Virtex 4 LX25 programmable structure. Data is stored in fast BRAM (Block-Random-Access-Memory) memory blocks during the measuring series, and then is copied to external DDRAM (Double-Rated-Dynamic-RAM). Simultaneously to the process of measuring data can be copied to the personal-computer by Ethernet interface.

Fig. 3 shows the construction details of TDL that has been used in TIMM design. This TDL block consists of carry-logic chain and register. The task of the register is to seize the TDL state when the START/STOP pulse appears.

Every CLB (Configurable Logic Block) consists of two configurable flip-flops/latches and fragment of the carry-logic chain. The carry-logic chain is the shortest and the fastest connection between TDL segments and D-inputs of flip-flops. This fact has been used for TDL construction. All the carry-logic elements have been connected serially - CLB nearby CLB. Unfortunately such easy connections are not sufficient for proper operation of priority code-converter. Here, standard-clock phase would be decoded improperly, because of different propagation time of START/STOP

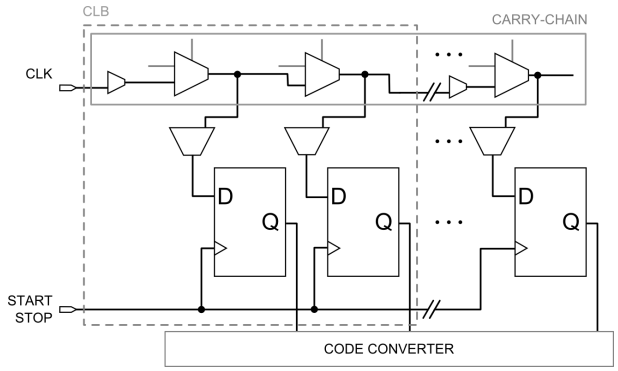

Fig. 3. Tapped-delay-line details.

signals within FPGA structure. That is why after the system calibration one has to rewire connections between D flip-flops outputs and priority code-converter inputs.

The standard-clock signal is connected to the TDL first segment input and START/STOP signal is connected to flip-flop clock inputs. During the event the START/STOP pulse appears and the TDL state is registered in flip-flops. The registered standard-clock signal is then transferred to priority code-converter in order to compress and convert the standard-clock phase value for the event.

The number of segments in every TDLs is equal to 210. The total delay of these segments is a little larger than the standard-clock period ($5\ ns$). For every TDL usually a few last segments are not used but they were implemented as a reserve because of standard-clock period fluctuations and delay fluctuations caused by temperature fluctuations or supply voltage fluctuations. On average 200 segments of TDL is used, so the average measure resolution is equal to about $\frac{5\ ns}{200} = 25\ ps$.

Fig. 5 shows TIs histograms obtained for different number of measure series (m) done by TIMM with different number of TDLs (n) (the product mn is constant and is equal to 3200). There are not visible differences between these histogram. They differ however in time needed to be devoted for measure procedure, that is 16 times less for TIMM equipped with 16 TDLs than for TIMM with single TDL. There are also differences in time of data transmission, that is exactly 6 times less for the TIMM equipped with 16 TDLs. Every 16 measurements consists of two 32-bit standard-clock counters values and 8 bits of standard-clock phase value ($2 \times 32 + 8 \times 16 = 192$) when TIMM with 16 TDLs is used. Whereas there are thirty two 32-bit standard-clock counters used when TIMM with single TDLs is used, the number of bits needed to code standard-clock phase is the same ($(32 + 32 + 8) \times 16 = 1152$), $\frac{1152}{192} = 6$. Standard-deviation of TIs whose histograms are shown in Fig. 5 are all equal to about 32 ps, then the standard deviation of their average-values are all equal to $\frac{32\ ps}{\sqrt{16}} = 8\ ps$.

Fig. 6a shows TI histograms obtained for 16 shots (16 measurements) in case when TIMM with single TDL is used. When TIMM equipped with 16 TDLs is used then these 16 shots are the equivalent of 256 measurements - the TI histogram (Fig. 6b) is then more the Gaussian one.

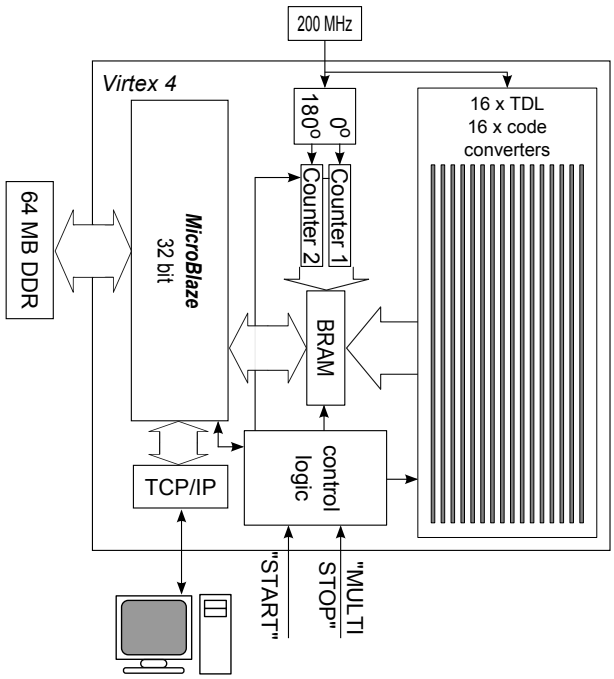

Fig. 4. The block diagram of time-interval-measuring-module equipped with sixteen tapped-delay-lines.

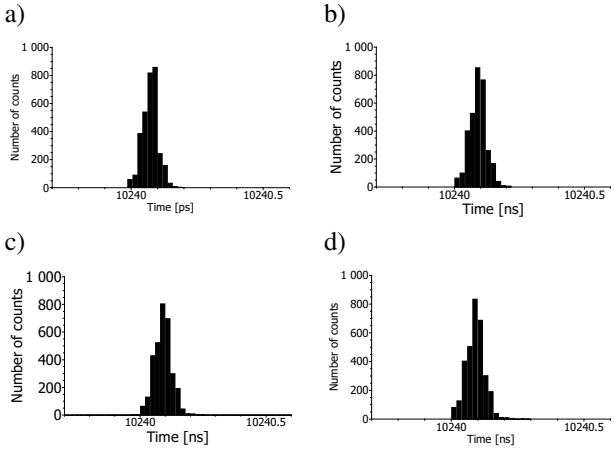

Fig. 5. Time-interval histograms measured by module equipped with (a) one, (b) four, (c) eight, (d) sixteen tapped-delay-lines, when (a) 3200, (b) 800, (c) 400, (d) 200 shots have been generated.

4. MAXIMAL MEASUREMENT INTENSITY INCREASE

Fig. 7 shows mainly modifications that have been done to obtain higher maximal intensity of registered TSs. Additionally to the solution presented in Fig. 2 components of the second stage U_2 have been added. The role of this stage components is to readout data produced by the first stage U_1 as quickly as possible. Having been read by stage

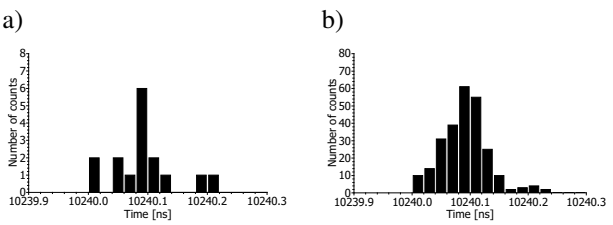

Fig. 6. Time-interval histograms measured by module equipped with (a) one and (b) sixteen tapped-delay-lines, when 16 shots have been generated.

U_2 components, the stage U_1 components are able to register new TSs.

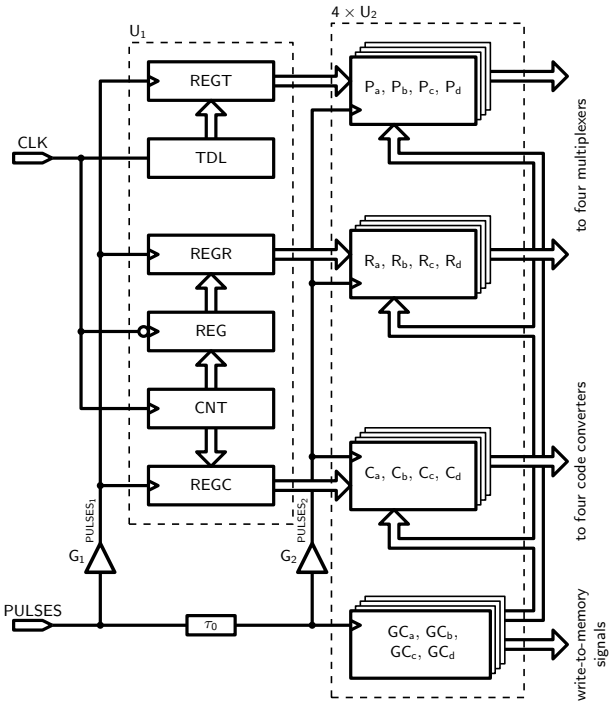

Fig. 7. Time-interval measuring module modified in respect of maximal intensity of registered time stamps.

The second stage U_2 consists mainly of registers that are controlled by Gray-code counters (GC_a, GC_b, GC_c, GC_d) in order to eliminate distortions. The Gray-code counters are responsible for pointing out the active triplet of registers (a, b, c or d). Registers (P_a, P_b, P_c, P_d) keep data read from TDL during code-conversion. Whereas registers (R_a, R_b, R_c, R_d) and (C_a, C_b, C_c, C_d) are responsible for storing data while the multiplexer chooses either register REG or counter CNT value (information about standard-clock period number value). Global buffers G_1 and G_2 are needed for fast signal connections to be used in FPGA in order to minimise clock-skew.

Fig. 8 shows idea of parallel data processing by stage U_2 components. Every group of registers (either a or b or c or d) is activated every fourth pulse, so the maximal-intensity of registered TSs is four times higher. Sometimes

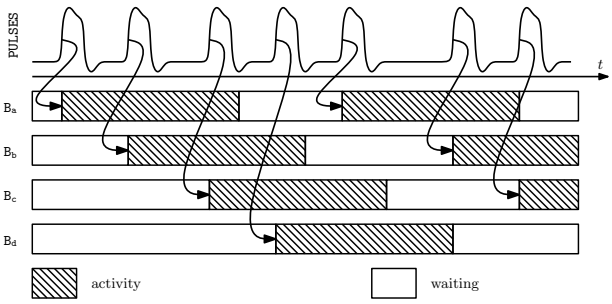

Fig. 8. The idea of parallel data processing.

to reduce code-conversion time one can modify conversion code construction to allow results in different code than natural-binary one or to not carry out conversion at all. However, such approaches would complicate further data processing.

In order to accelerate the process of conversion every TDL possesses its own code-converter and the code-conversion can be a two stage-process. In the first stage the code is converted with the use of four independent code-converters. At this stage every code-converter translates 16-bit thermometric code to 4-bit natural-binary code and then the result is written into internal BRAM (Fig. 4). The second stage is done during transfer from BRAM do the external DDR (Fig. 4). The final standard-clock phase information for every event per one TDL is coded in 6-bit natural-binary code.

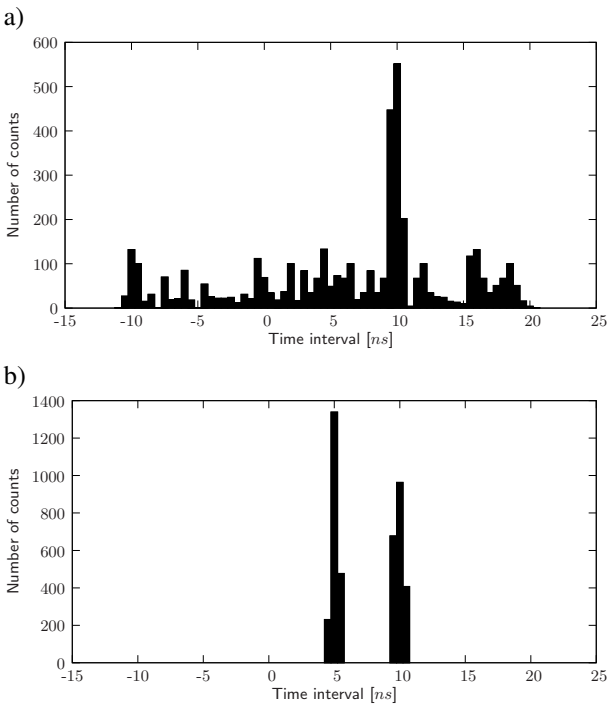

Fig. 9. Measured time-interval histograms for patterns (TSs of 5 ns and 10 ns) in case when (a) no parallel data processing has been used and when (b) data processing has been paralleled.

Fig. 9 shows measured TI histograms obtained for pattern that consists of $5\ ns$ and $10\ ns$ TIs depending on parallel processing has not been used (Fig. 9a) or has been used (Fig. 9b). The maximal intensity of registered TSs of TIMM with single processing path (Fig. 2) that has been implemented into Virtex XCV300 is equal to about $125\ MHz$ (dead-time is equal to $8\ ns$). TSs that create the endings of TIs that are shorter than $8\ ns$ are not then properly converted and stored (Fig. 9a). Apart from the clearly visible peak at the position of $10\ ns$ there is a lot of noise.

When the maximal intensity of registered TSs is sufficient (9b) then the histogram contains both peaks. All the measurement are contained in either one or in the other peak - the noise is not present at all. Here, the estimated maximal intensity of registered TSs is equal to about $225\ MHz$ - dead-time is less that $4.5\ ns$.

Please notice that the peak in Fig. 9a is also shorter that the equivalent one in Fig. 9b. This happens because the ending of $5\ ns$ TI is at the same point that the beginning of $10\ ns$ TI. So both ones are dispersed but not equally. The $5\ ns$ peak is dispersed completely because every TS that corresponds to $5\ ns$ TI ending is missed. The $10\ ns$ peak is missed partially. Only those $10\ ns$ TIs that are preceded by $5\ ns$ ones are incorrect.

5. CONCLUSIONS

Two methods of improving metrological parameters of TIMS have turned out to be very successful. The implementation of 16 TDLs allowed increasing the uncertainty 4 times. The presented method allows obtaining the same results in more than 16 times shorter time. The implementation of the second stage of processing allowed increasing the maximal intensity of registered TS from $125\ MHz$ to $225\ MHz$. Both improvements have been implemented into two different FPGA structures (Virtex and Virtex 4). However these improvements can easily be ported to other FPGAs.

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