SIMULATION OF THE "SINGLE VIA THERMAL CYCLE TEST" FINITE ELEMENT MODELLING OF PCBS UNDER THERMAL LOADS

K. Fellner [1] **, P. F. Fuchs** [2] **, G. Pinter** [3]

Summary: *The "Single Via Thermal Cycle Test" (SVTCT) is a thermal cycle test used for life time assessment of Printed Circuit Boards (PCBs) under cyclic thermal loads. During the SVTCT, the electrical conductivities of the interconnections (vias) of the tested PCB are monitored by resistance measurements. Hence, by a decrease of electrical conductivity, failure can be detected. A single via in a PCB is modeled using an axisymmetric simulation model. The simulations are conducted decoupled. One model for computing the temperature field in the PCB and another model to compute the stress and strain distribution are generated. The calculated stress and strain distributions are opposed to microsections of vias in PCBs, which have been subjected to the SVTCT. All cracks occurred at locations, which are highly stressed according to the simulations. This research work is part of the Master's Thesis "Simulation of the 'Single Via Thermal Cycle Test' - modelling and determination of the material input parameters" citebib1.*

Keywords: *printed circuit board, interlayer connection, copper, prepreg, thermal expansion, finite element simulation, decoupled simulationm*

1 Introduction

The aim of this research work is the life time assessment of Printed Circuit Boards (PCBs) under cyclic thermal loads. PCBs are subjected to thermal loads for example in motor control systems or during the production process of the PCB. Hence the behavior of PCBs under thermal loads needs to be known and for that reason the "Single Via Thermal Cycle Test" (SVTCT) is performed. A thermal cycle test [2, 3] is a testing method for printed circuit boards, which is typically carried out in a two-chamber system. In one of the chambers a low temperature (typically -55 °C to -40 °C) and in the other chamber a high (typically 125 °C to 150 °C) temperature is set. The board under test is transported in a basket from chamber to chamber. So, the temperature change is very fast and the time spent in a chamber is typically 15 to 30 minutes. In the SVTCT the vias of the tested PCB are monitored by resistance measurements. If a significant increase of the electrical resistance is recorded, the conductive connection is broken and the end of product life is indicated. To reduce the effort for testing and to save the associated costs, Finite Element Analyses (FEA) are performed. This paper deals with FEA modelling of a single via in a PCB tested in the SVTCT. The needed material input data for the simulations, the heat capacity, the density, the linear thermal expansion coefficients and the mechanical properties were obtained using suitable testing methods. The testing and the corresponding results are described in [1]. Copper and FR4-prepregs (glass fiber reinforced epoxy resin) were tested. The work shown in this paper is part of the Master's Thesis "Simulation of the 'Single Via Thermal Cycle Test' - modelling and determination of the material input parameters" [1].

[1]Klaus Fellner, Polymer Competence Center Leoben, 8700 Leoben, Austria, email: klaus.fellner@pccl.at
[2]Dr. Peter Filipp Fuchs, Polymer Competence Center Leoben, 8700 Leoben, Austria
[3]Prof. Dr. Gerald Pinter, Institute of Materials Science and Testing of Polymers, Montanuniversitaet Leoben, Austria

2 Methodology

Figure 1a shows a micrograph of a single via in a PCB, Figure 1b shows the corresponding axisymmetric FEA model generated in the FEA software Abaqus (Abaqus 6.11, Simulia, Daussault Systèmes, Vélizy-Villacoublay, France). In the micrograph, the copper in the via is easily visible. PCBs containing vias with

a) b)

Figure 1: a) Micrograph of a via, b) FEA model in Abaqus [1]

different diameters and thicknesses of the copper plating inside the via (see Table 1) where produced and tested in the SVTCT, corresponding FEA models were created.

Table 1: Overview of the different designs for the SVTCT. In brackets the average thickness of the copper plating is given. [1]

Diameter of the via [mm]	$0,25$	$0,3$	$0,5$	$0,8$	$1,0$
Setting A (34,6 μm)	$A-0,25$	$A-0,3$	$A-0,5$	$A-0,8$	$A-1,0$
Setting B (51,8 μm)	$B-0,25$	$B-0,3$	$B-0,5$	$B-0,8$	$B-1,0$

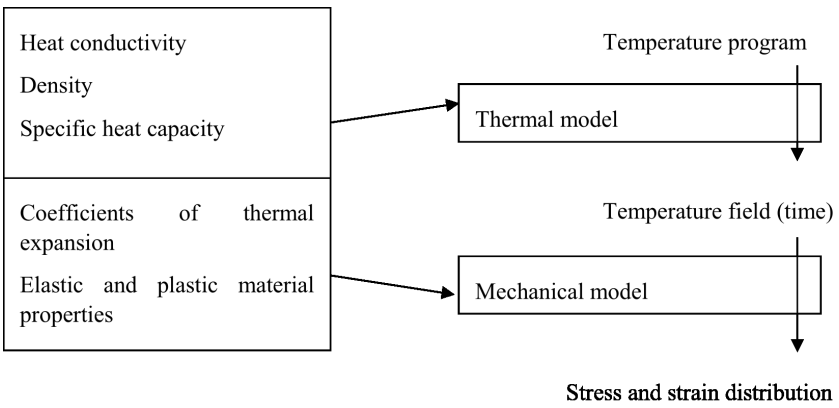


Figure 2: Procedure for the decoupled simulation of a PCB in the SVTCT. [1]

The heating up from 25 °C to 125 °C is simulated and the stresses and strains at this temperature is evaluated, since the thermally induced stresses are at their peak at the highest temperature. The simulations are carried out decoupled, a model for calculating the temperature field and another model to calculate the stress and strain distribution were applied. Figure 2 depicts the approach.

Both models have the same geometry and use the same material input data. They only differ in the element type applied. The thermal model uses elements (Abaqus name DCAX8) which are able to calculate the temperature field. Therefore, the heating up from 25 °C to 125 °C is specified on the free surface of the thermal model and the resulting temperature field inside the model was calculated. In the mechanical model elements (Abaqus name CAX8R) suitable for stress-strain analysis are employed. It uses the information about the time-dependent temperature field and calculates the thermally induced stresses and strains. Resulting data

3 Results and Discussion

In this section the results of the FEA simulations and micrographs of specimens, tested in the SVTCT are compared. Figure 3 shows the Mises equivalent stress distribution and the equivalent plastic strain distribution (Abaqus name: PEEQ) for the setting A-0,25. Figure 4 shows the location of cracks found in micrographs

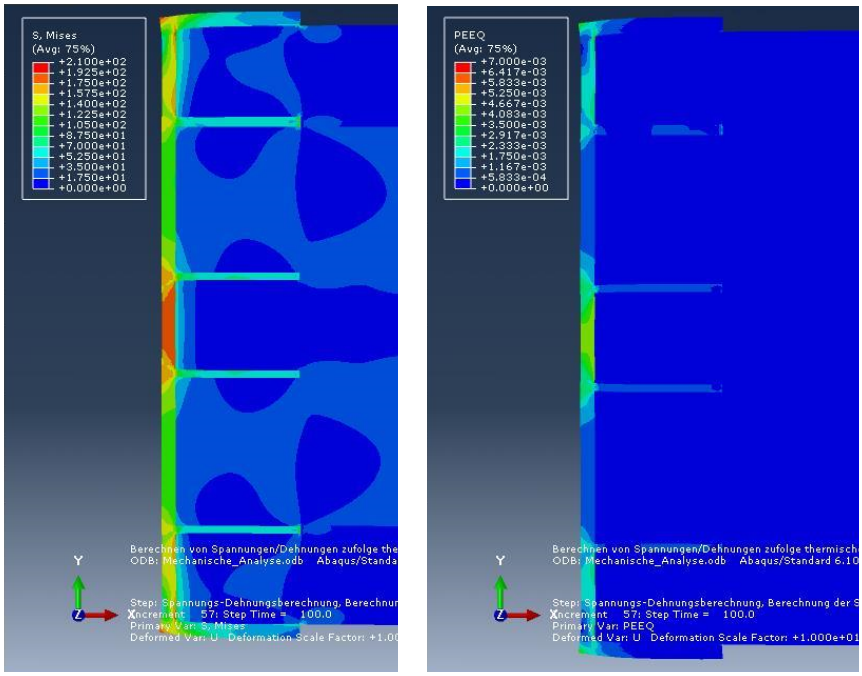


Figure 3: Stress and strain distribution, setting A-0,25. [1]

of the corresponding specimens. All of them occurred in the highly stressed area in the middle of the via, as predicted by the simulations, see Figure 3. Generally the stresses in the middle of the via decrease at higher diameters of the via. Figure 5 shows that dependency, the stress values were taken from a reference element in the middle of the via, which is also shown in Figure 5. Moreover, a thicker copper plating also reduces the stresses and so the probability of failure. Although these simulations do not contain any failure hypotheses, they allow a qualitative comparison of the occurring stresses and strains in the different setting during the SVTCT. Thus, conclusions can be drawn on the performance. Cracks in the experiments occurred at those sites that have been identified by the simulation to be highly stressed.

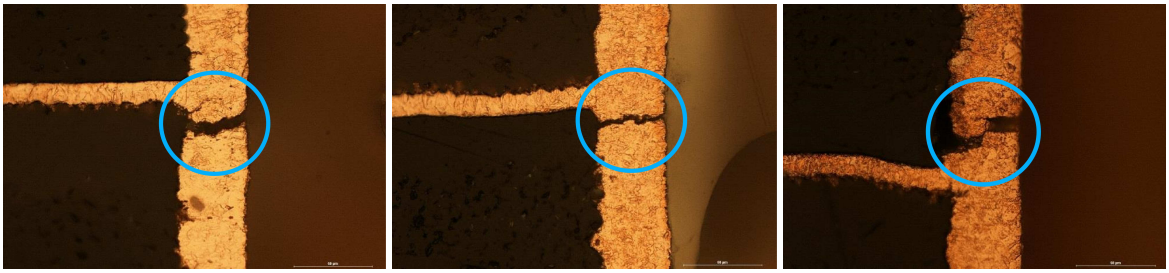
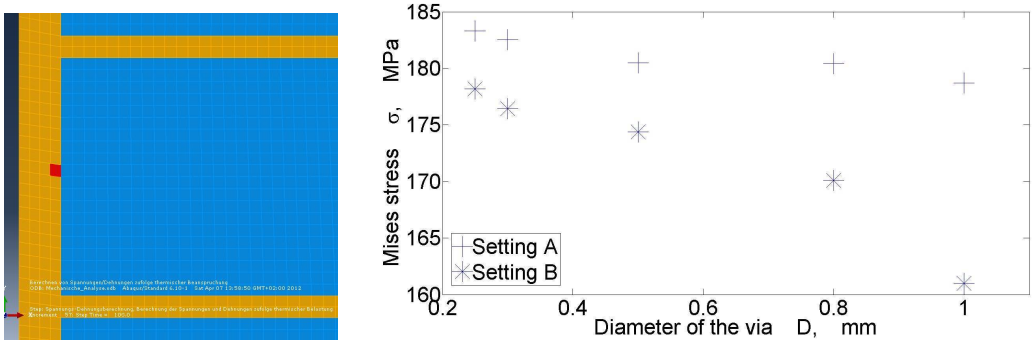


Figure 4: Cracks in specimens of the setting A-0,25. [1]



a) b)

Figure 5: a) Reference element in the middle of the via marked in red (the copper layers are marked in orange), b) Mises stress over diameter of the via [1]

4 Acknowledgment

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